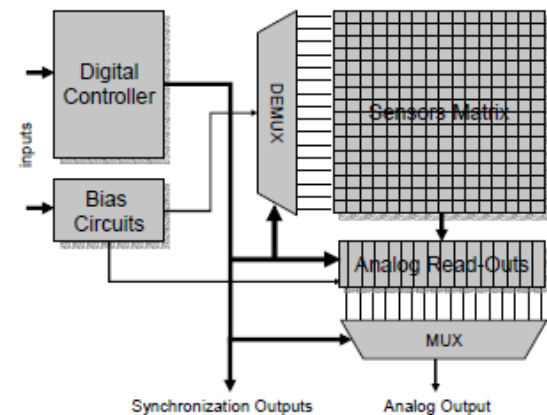


# CMOS–SOI–MEMS Transistor (TeraMOS) for Terahertz Imaging

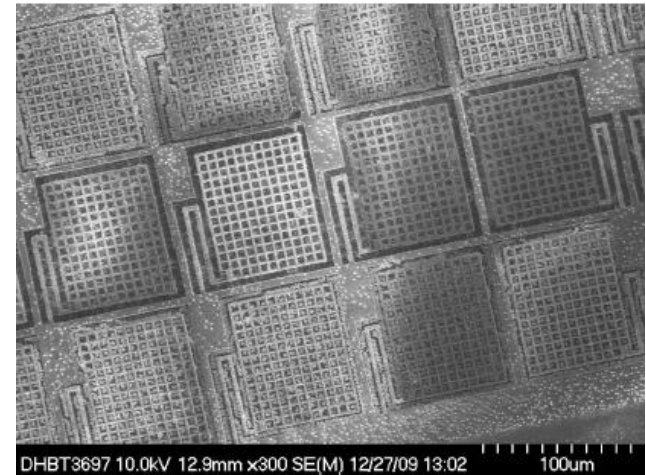
D. Corcos, D. Goren, Y. Nemirovsky

- ▶ Research Goal: to design a passive imager for the THz waves
- ▶ Specifications:
  - Wavelength 200–600  $\mu\text{m}$  (range 0.5–1.5 THz)
  - Video frame rate  $\sim$ 20–60 ms
  - High sensitivity: NETD < 1K
  - Monolithic FPA and read-out design



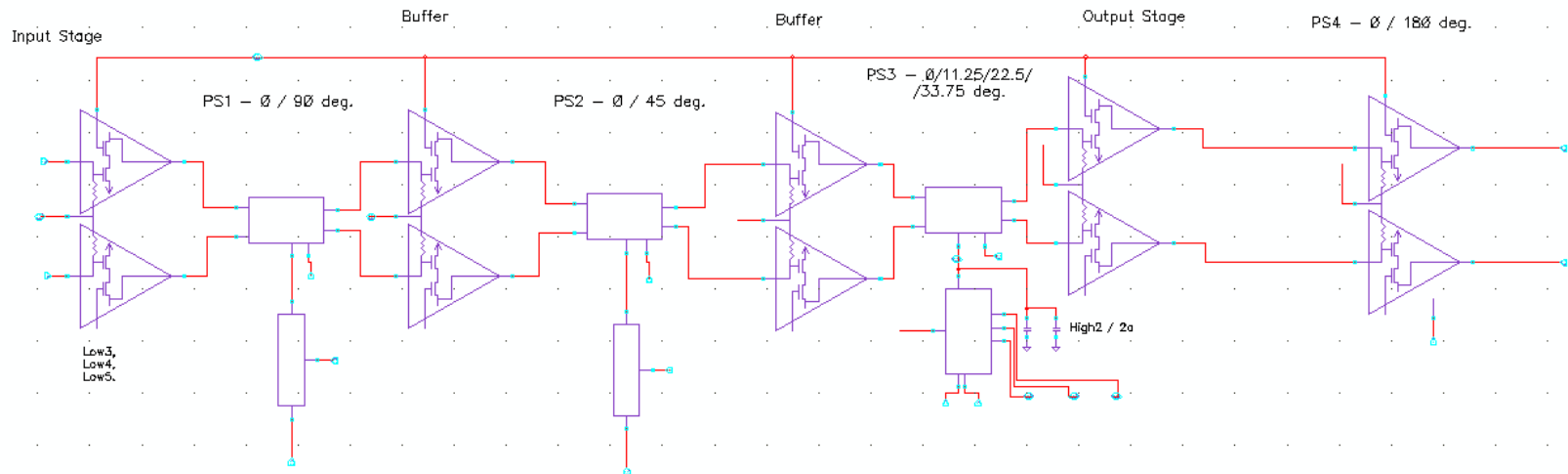
# CMOS-SOI-MEMS Transistor (TeraMOS) for Terahertz Imaging

- ▶ Proposed sensing element:  
a suspended MOS transistor, thermally isolated by micromachining (MEMS), and operated in sub-threshold; EM coupling achieved with direct absorber or integrated antenna
- ▶ Expected performance:
  - NEP=5pW, NETD=1K
  - TCC=4.5 %/K (measured)  
with 0.02 %/K<sup>2</sup> variation
  - absorption efficiency  $\eta=90\%$
- ▶ Research program for 2010:
  - Optical characterization of the first design
  - Production of an optimized device



# Design of CMOS Phase Shifter, Gal Segev, I. Brouk, Y. Nemirowsky

- ▶ Specifications:
  - 360° coverage with 5 bits
  - working frequency: 12.5GHz
  - Bandwidth: 1GHz
- ▶ Main goal: design on Tower's process – 0.18 $\mu$



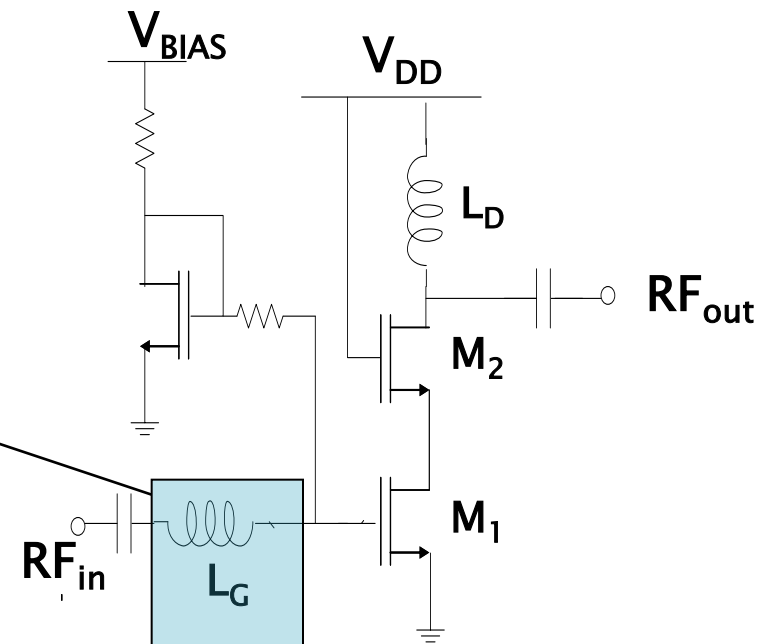
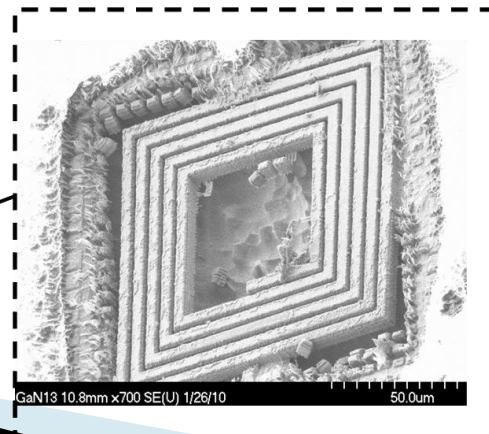
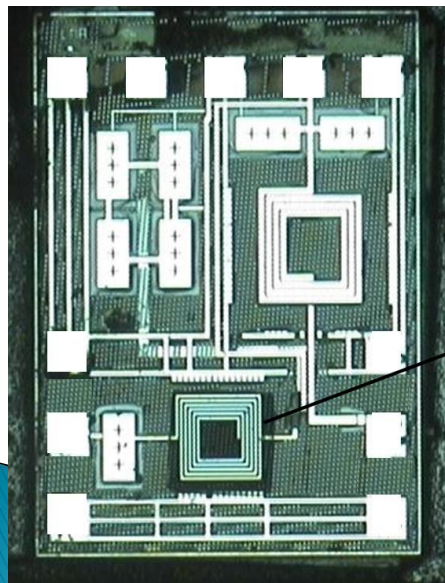
# Achievements and Broadcast

- ▶ Results of our design:
  - Area: 3X3 mm<sup>2</sup>
  - Losses: -0.3 dB
  - Gain Variation:  $\pm 0.4$  dB
  - Phase Error:  $< 0.4^\circ$
  - Temperature range:  $-20^\circ \div 80^\circ$
  - Ability to re-calibrate the PS after production.
- ▶ PS is now on fabrication.  
Measurements will be held on its return.

# A CMOS Low Noise Amplifier with Integrated Front-Side Micromachined Inductor

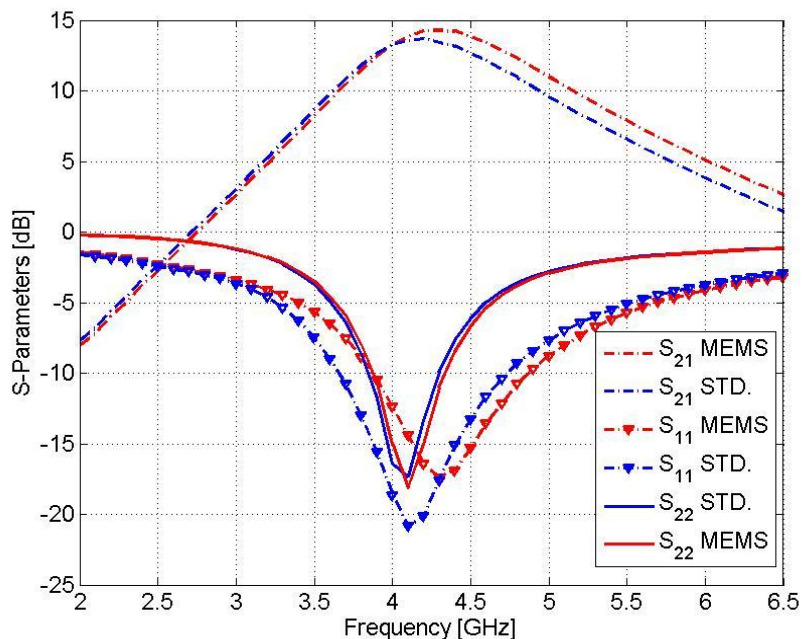
R. Ben-Yishay, S. Stolyarova and Y. Nemirovsky

- ▶ RFIC inductors performance are improved by a selective removal of surrounding silicon and oxide.
- ▶ **Main goal:** Study of post-processing effects on active CMOS circuit performance

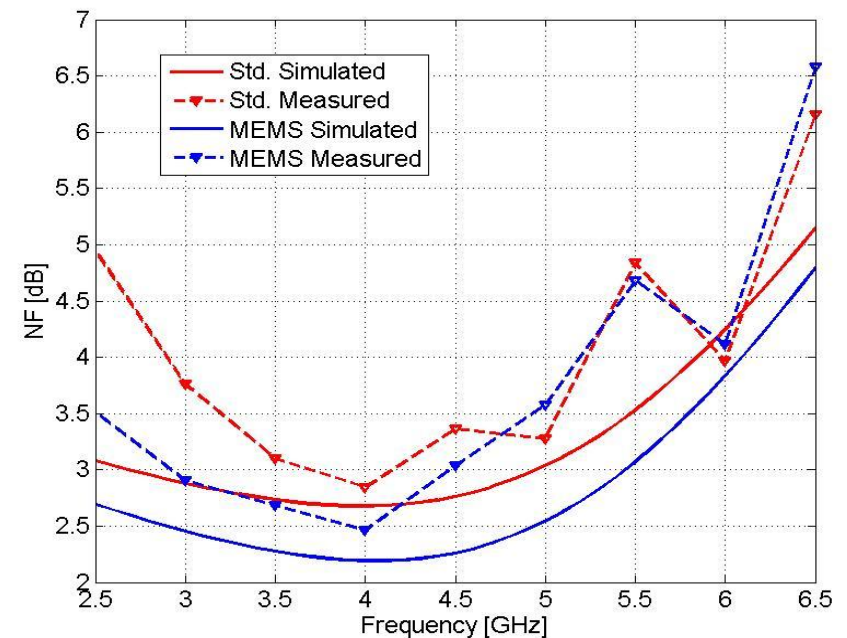


- ▶ Case study – 4GHz CMOS LNA fabricated in Tower 0.18 $\mu\text{m}$
- ▶ Low cost CMOS compatible post processing technique was applied on the inductor in the input matching network.
- ▶ Measurement results:
  - NF improvement of 0.5dB
  - Gain enhancement of 1dB
- ▶ Paper submitted to IEEE Electron Devices Letters

Measured S-parameters



Measured & Simulated Noise Figure

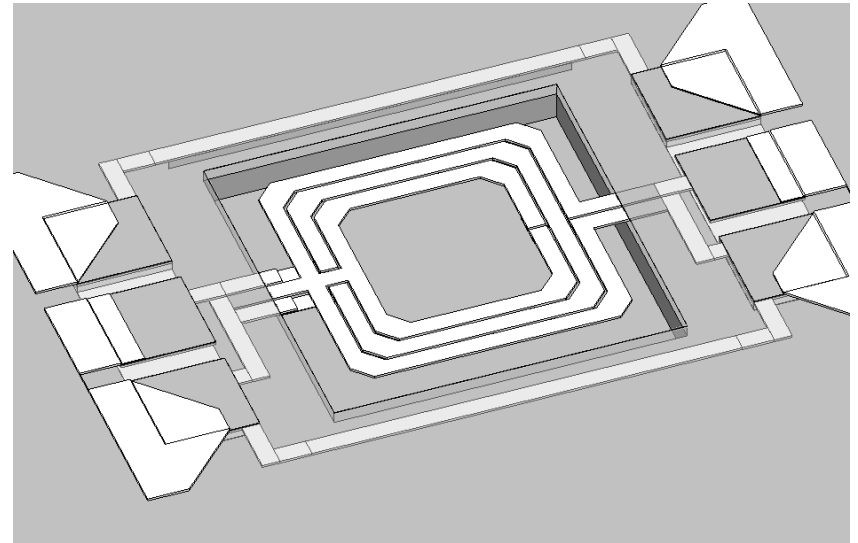


# High Performance MEMS 0.18 $\mu\text{m}$ RF-CMOS Transformers

*Shlomo Katz, I. Brouk, S. Stolyarova, S. Shapira, Y. Nemirovsky*

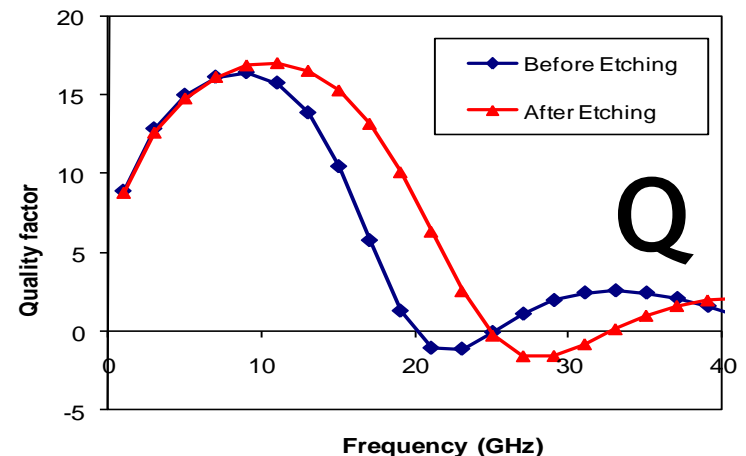
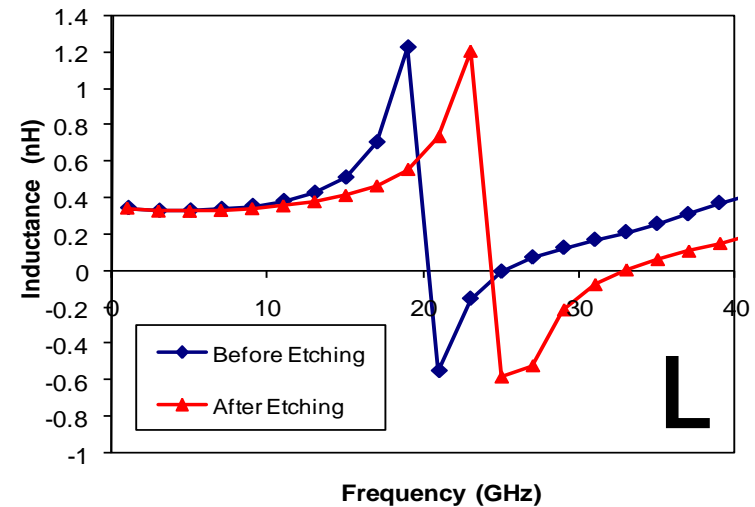
---

- ▶ **Background:**
  - Inductor/transformer parasitic elements: C, R
  - Parasitics cause self-resonance and limit Q
  - Removing oxide/substrate material decreases parasitics
- ▶ **Main goal: Improve transformer performance with MEMS post-processing**



# Results and Achievements

- ▶ Results of our design:
  - Peak Q and self-resonant frequencies increased by over 20%
  - Insertion loss and cross-talk reduced
- ▶ Results pictured are from HFSS simulations. Devices recently returned from fabrication; measurements will be performed after post-processing .





# FOX: Fast on-chip Interconnect

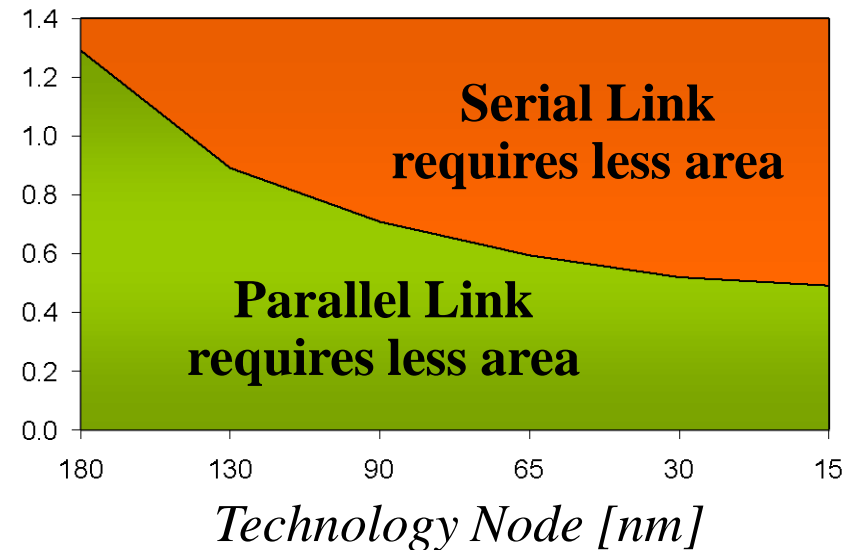
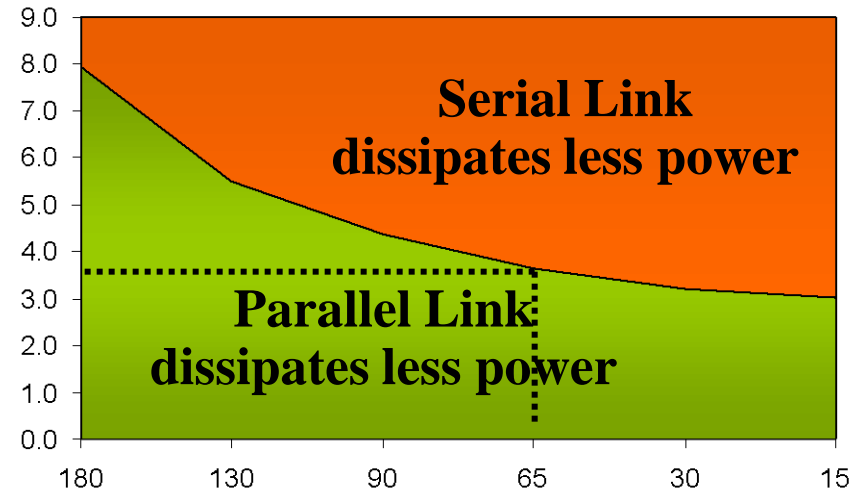
*Very high speed on-chip serial  
interconnect*

Dr. Reuven Dobkin  
Prof. Ran Ginosar  
Prof. Avinoam Kolodny

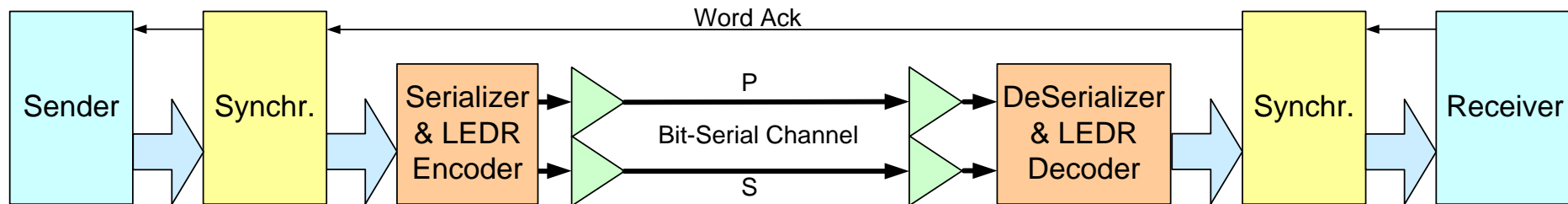
# Serial Link Employment Benefits

- ▶ Why Serial Link?
  - Less interconnect area
  - Less routing congestion
- ▶ Less coupling
  - Less power (depends on range)
- ▶ The relative improvement grows with technology scaling

*Link Length [mm]*



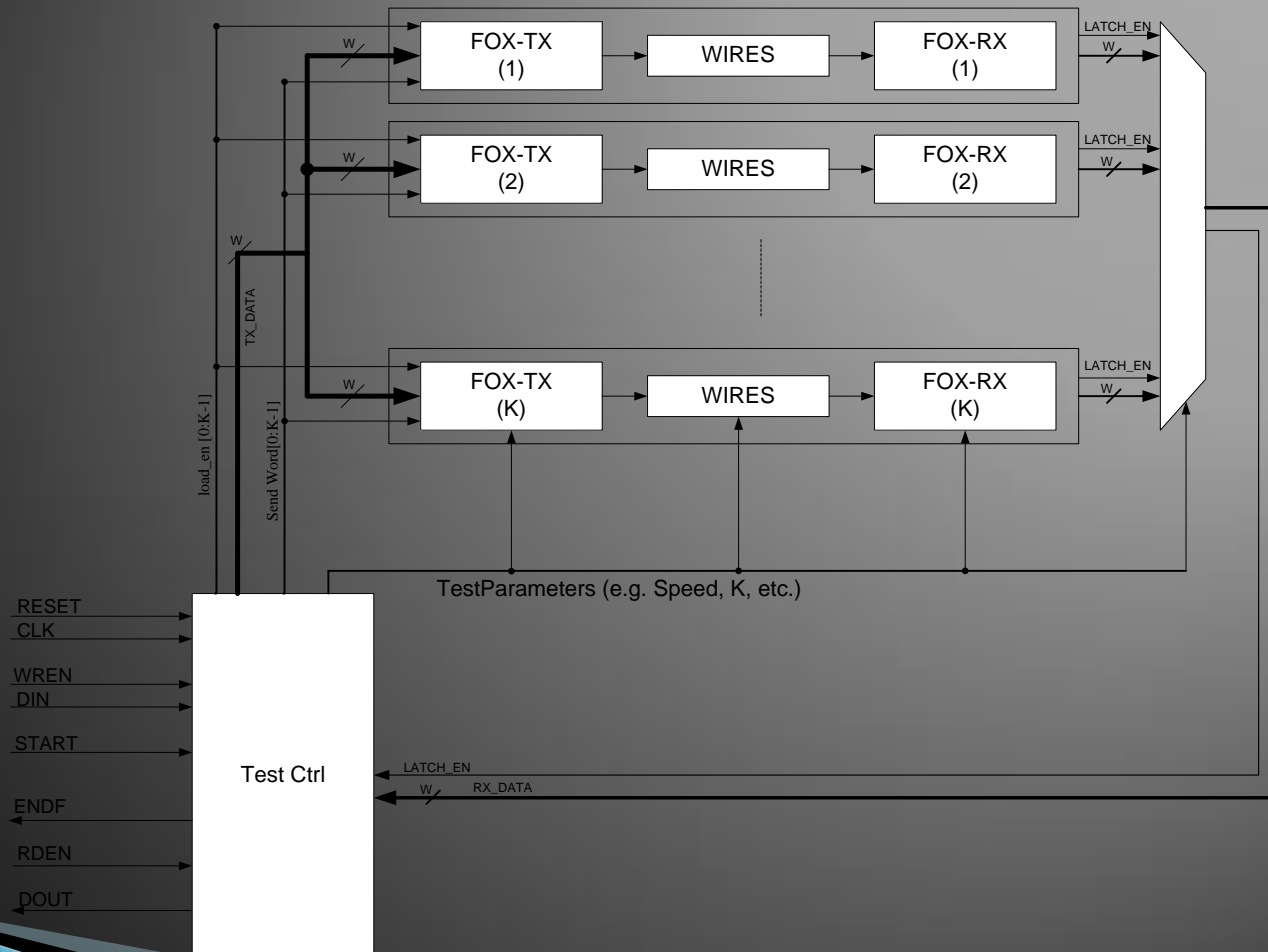
# Serial Link Structure



- ▶ Transition signaling instead of sampling: two-phase NRZ Level Encoded Dual Rail (LEDR) asynchronous protocol, a.k.a. data-strobe (DS)
- ▶ Acknowledge per word instead of per bit
- ▶ Wave-pipelining over channel
- ▶ Differential encoding (DS-DE, IEEE1355-95)
- ▶ Low-latency synchronizers
- ▶ **Single gate delay data cycle (faster than anyone else)**
  - 67Gbps @ HP65nm

# FOX test-chip (fabrication in 2010)

Link Architecture (only one is active per a time)



# FOX: Fast on-chip Interconnect

*High speed, Current mode serial  
interconnect*

Danniel Nahmanny  
Prof. Ran Ginosar

# Goals

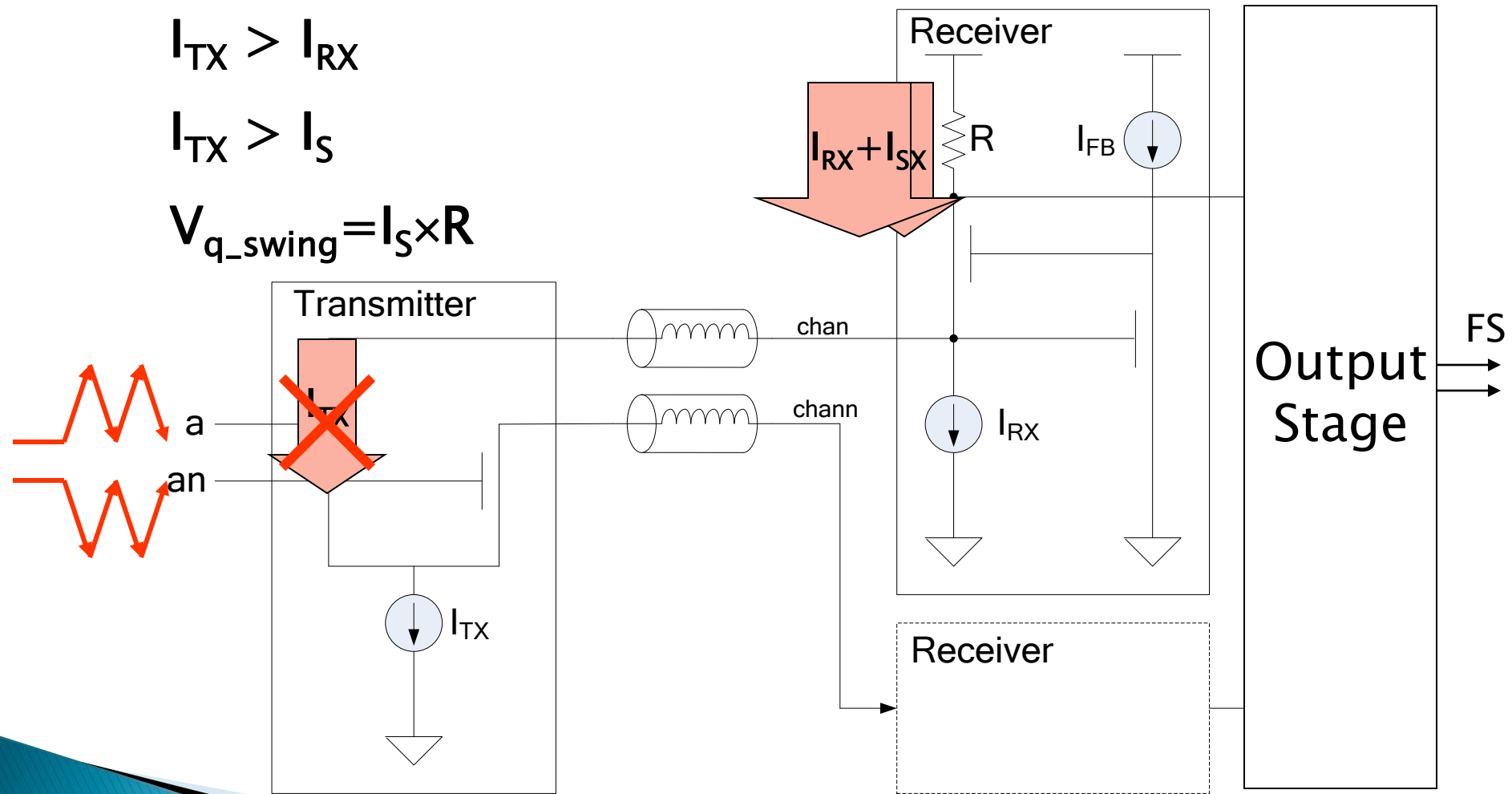
- ▶ Full Current Mode:
  - Send current from TX
  - Measure current at RX
- ▶ Minimal voltage swing over channel
- ▶ Current to voltage conversion at RX
- ▶ Long range repeater-less channel
- ▶ Targeted data cycle 15 ps (67 Gbps) @ 65nm
- ▶ Low power

# Differential Channel Driver and Receiver

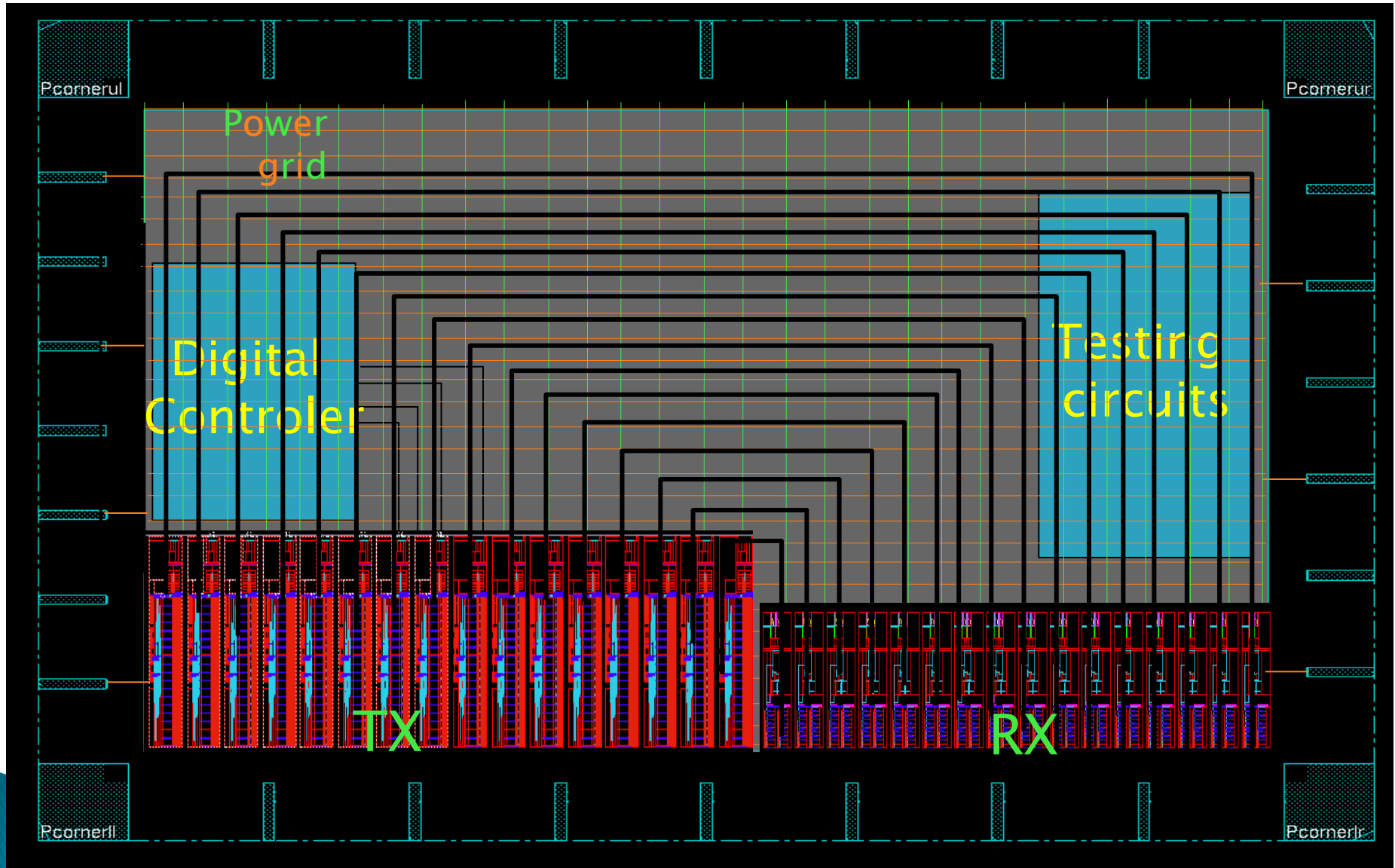
$$I_{TX} > I_{RX}$$

$$I_{TX} > I_S$$

$$V_{q\_swing} = I_S \times R$$



# FOX chip structure

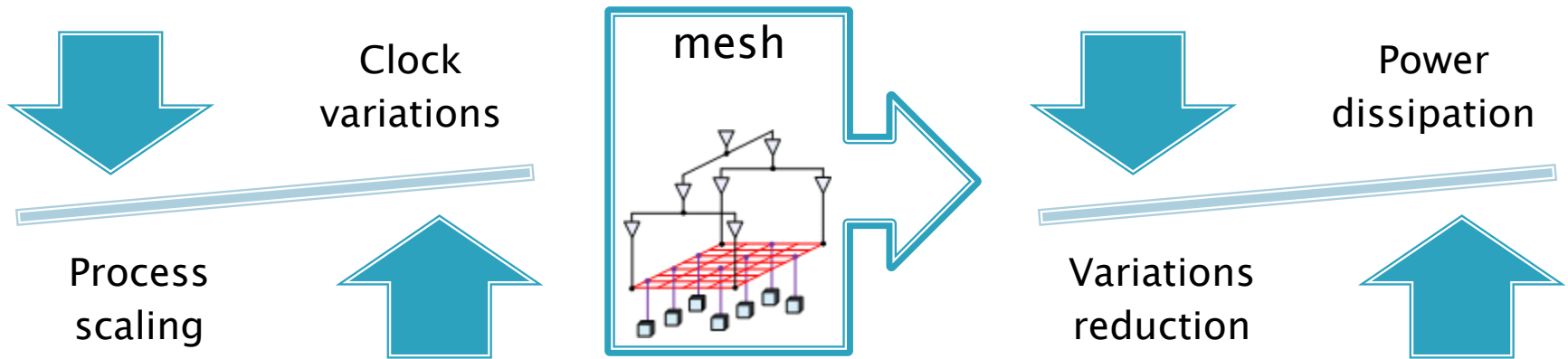




# Timing-Driven Variation-Aware Nonuniform Clock Mesh Synthesis

Ameer Abdelhadi, Ran Ginosar, Avinoam Kolodny, and Eby G. Friedman

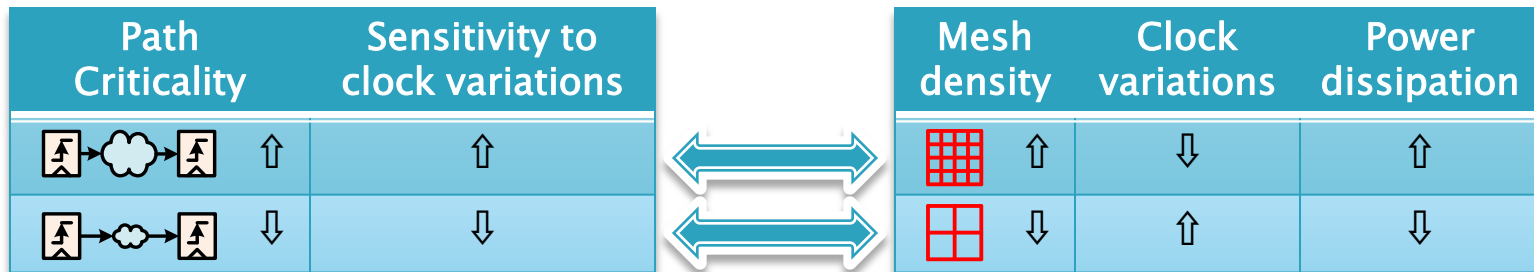
## Motivation



**Goal:** reducing clock skew variations while keeping minimal power dissipation overhead

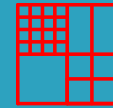
# Timing-Driven Variation-Aware Nonuniform Clock Mesh Synthesis

## Method



- Path criticality prioritization
- Managing skew tolerance

Nonuniform  
clock mesh

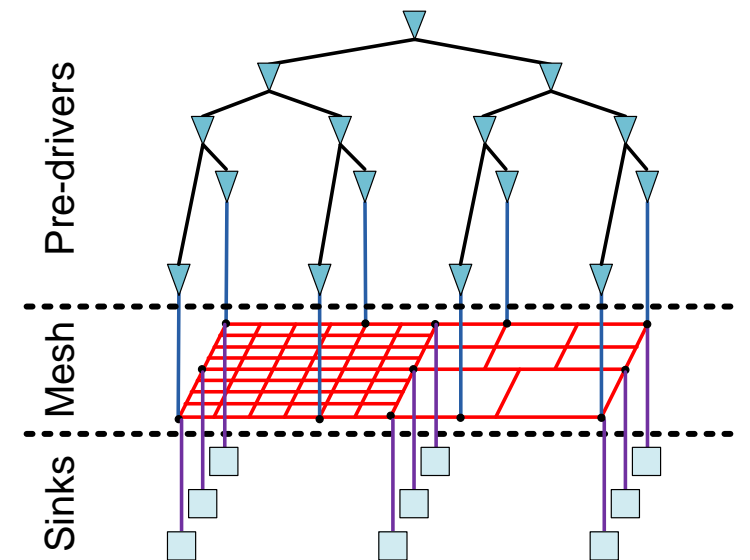
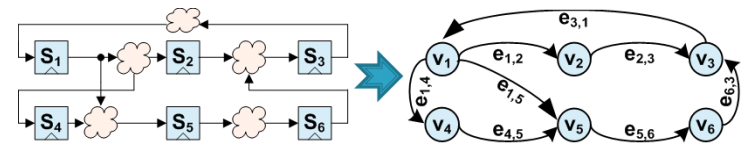


Selective reduction of clock skew variations based  
on circuit timing criticality

# Timing-Driven Variation-Aware Nonuniform Clock Mesh Synthesis

## Implementation

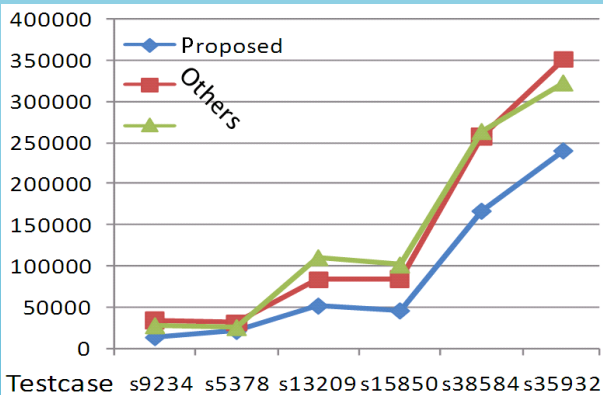
- ▶ Algorithms:
  - Graph-theoretic
    - for timing constraints
  - Geometric
    - for LO generation
- ▶ Quasi-linear ( $n \log n$ ) runtime
- ▶ Design Environment:
  - RTL to layout design flow
  - Standard EDA tools
  - Standard 65nm library
  - ISCAS89 benchmarks



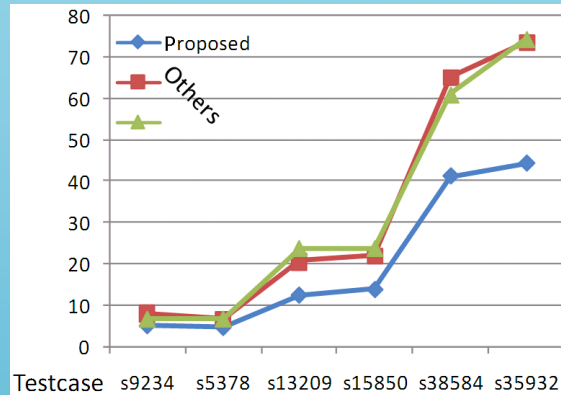
# Timing-Driven Variation-Aware Nonuniform Clock Mesh Synthesis

## Results

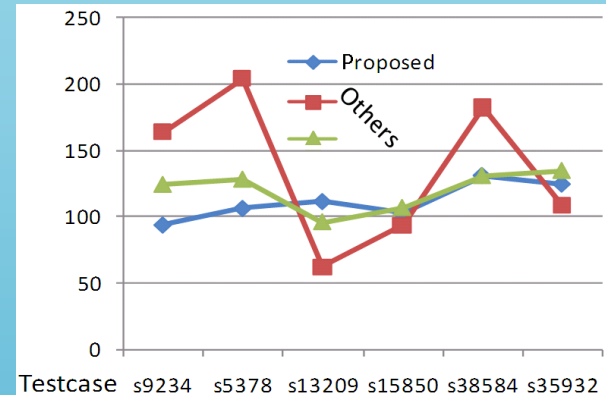
### Wire length (um)



### Power (mw)



### Maximum skew (ps)

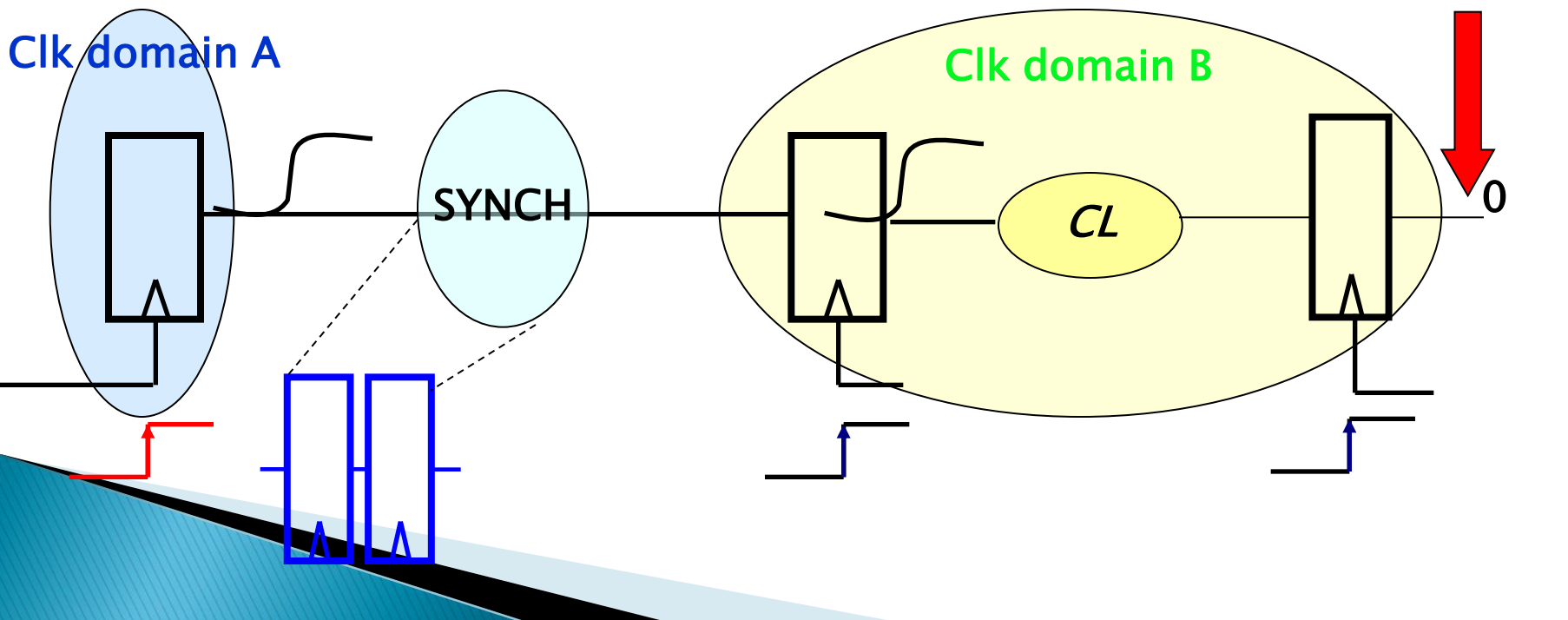


37% average reduction in metal  
39% average reduction in power dissipation

# Synchronizers degradation with scaling

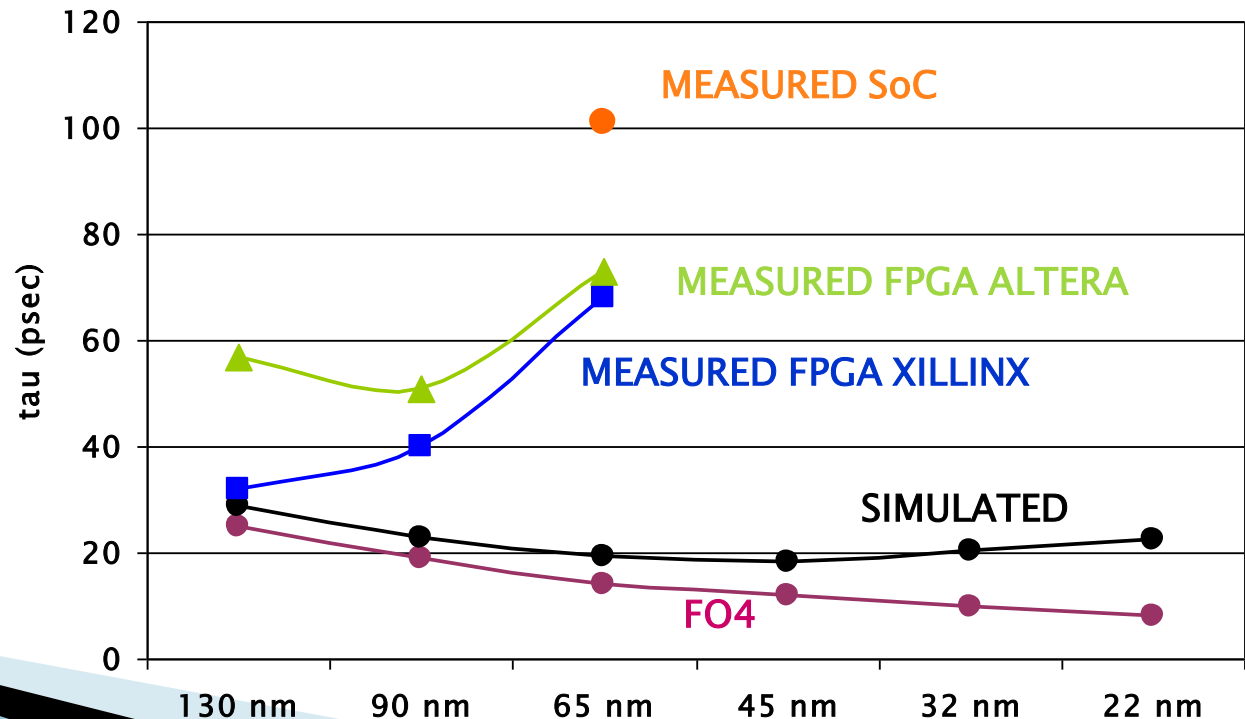
*Shlomi Beer, Advisor: Prof. Ran Ginosar*

- ▶ Circuits and SoCs employ multiple clock and voltage domains. Communication between different modules may lead to metastability.
- ▶ Metastability produces “esoteric” behavior in FF output. (increased delay)
- ▶ Metastability may lead to fatal errors.



# Findings and Results

- ▶ Synchronizer performance is measured by its recovery time
  - Fast recovery → Good synch. Slow recovery → Bad synch
- ▶ Recovery time of synchronizers ( $\tau$ ) was believed to scale with technology.
- ▶ We found that  $\tau$  degrades with scaling....



# Research program for 2010

## ▶ Why ?

- Identify physical causes of the degradation effect

## ▶ How?

- Refine the metastability model

## ▶ Can we fix it?

- Develop circuits to mitigate the degradation effect

# High performance computing in power and thermal constraint environment

Efi Rotem

Primary advisor: Ran Ginosar

Co advisors: Uri Weiser, Avi Mendelson

Masters work published at Micro-42

Continuing with PhD research



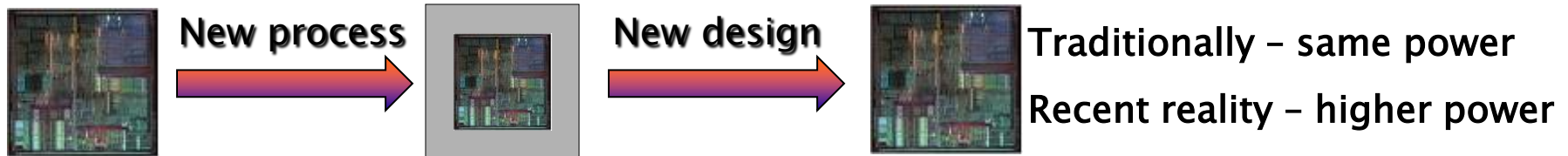


# The power wall is here – call for action

$$\text{Power} = C * V^2 * F + \text{Leakage}$$

## ▶ Scaling of new Process technology:

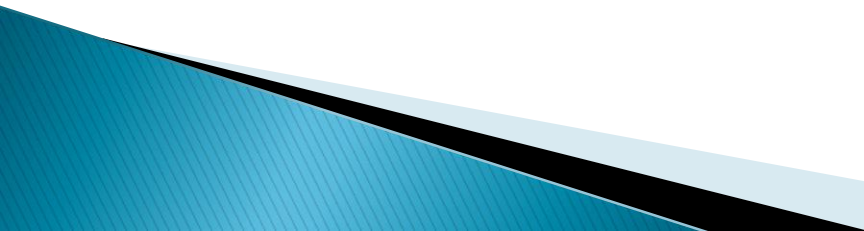
- Linear Dimensions: Shrinks by 0.7
- Area: Shrinks by  $0.7^2$
- Capacitance: Shrinks by 0.7 (1.4X capacitance density)
- Frequency: Scale up by 1.4 (Lower scaling due to RC)
- Voltage: Scale down by 0.7 (Not scaling any more)



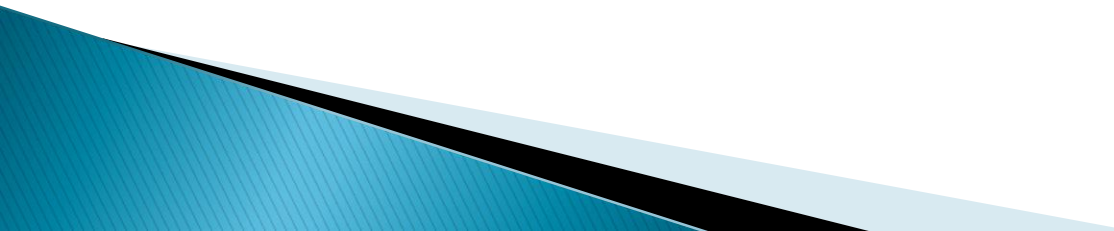
- **Industry is already in the power wall for almost a decade**
  - Continuously operating lower in the voltage range
  - Soon nominal voltage will equal min voltage

Compute performance roadmap is not sustainable any more

# Other “Mega” Trends

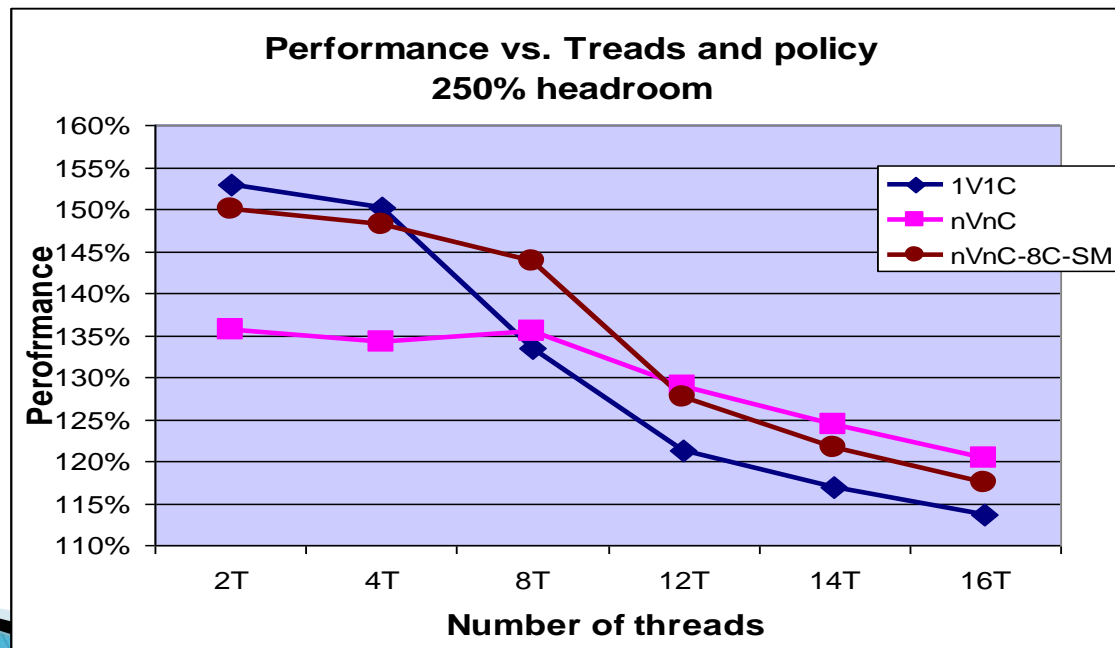
- ▶ Inside the chip:
    - Many cores – the dominant architecture
    - Migration of work to GP–GPU
    - Constraining physical parameters
      - Power, thermal, power delivery, process variability...
  - ▶ Out of the chip:
    - The importance of power and energy in the data rack and the data center
  - ▶ Resulting in increasing power and performance dynamic range
  - ▶ The key for performance under physical constraints → Management
- 

# Our research directions

- ▶ How to best architect and manage a high performance CPU in order to:
  - ▶ Extract maximum performance within physical constraints
  - ▶ Optimize energy at performance constraints
- 

# Micro-42 paper

- ▶ DVFS – A tool for power/perf. Management
- ▶ Introduced power delivery as a major constraint
  - Findings contradict some of previous studies
- ▶ Proposed clustered topology



# Millimeter wave circuits and phase array systems in CMOS process

**Emanuel Cohen**

**Supervisor : Dan Ritter**

**In cooperation with Intel**



# Goals and challenges of the research

## Goals

- ▶ Design full phase array CMOS system in 60GHz – For  $>5\text{Gb/s}$  data rate at  $\sim 10\text{m}$  range with power consumption  $< 1\text{Watt}$  size  $< 20\text{mm}^2$
- ▶ Current circuit designs for mm-Wave result in power consumption greater than few Watts / size  $> 100\text{mm}^2$ , for  $N > 30$  element array
- ▶ Analyze new architectural concepts and circuits design tradeoffs to meet power/size targets for mobile commercial application
- ▶ Examine innovative ways to benefit from CMOS integration and digital potential to create new systems in this area

## Challenges

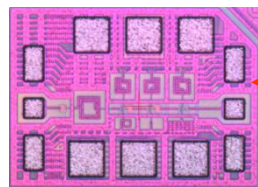
- ▶ Understand CMOS process advantages and limitations for mm wave use
- ▶ Circuit design at high freq close to  $F_{\text{max}}$  raises many research challenges on topologies and system performance



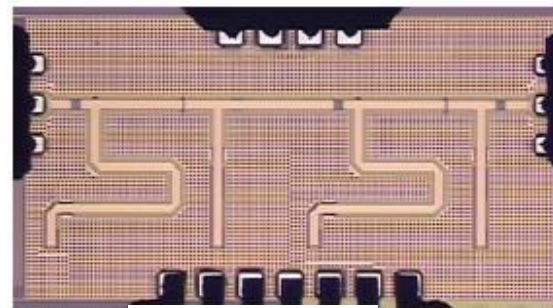
Create the basics for small low power fully integrated phase array system

# First research step (completed)

- ▶ Analysis of a phase array system – **understand the limitations for the smallest and most efficient system possible.**
- ▶ Flow definition for design and models for the basic passives and transistors in CMOS mm
- ▶ Design building blocks : LNA, PA, switches, phase shifters, mixers and combiners
- ▶ Design arrays : 4 element array, 32 element array + bump transition simulations and test structures
- ▶ Test measurement and investigation of all blocks



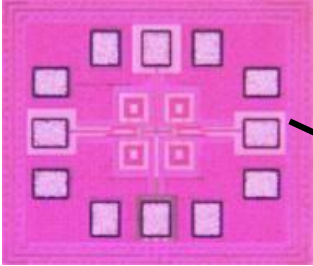
Inductor design



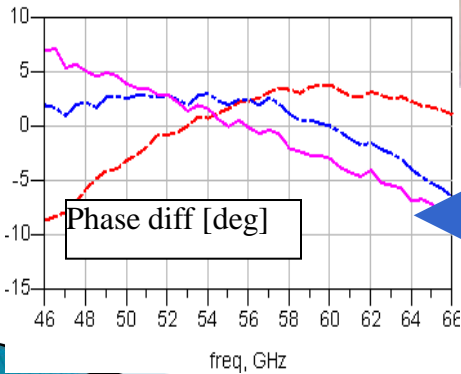
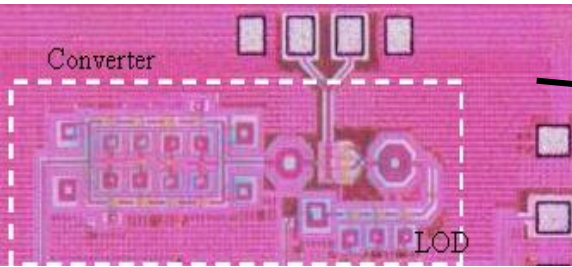
TL design

# Circuits design

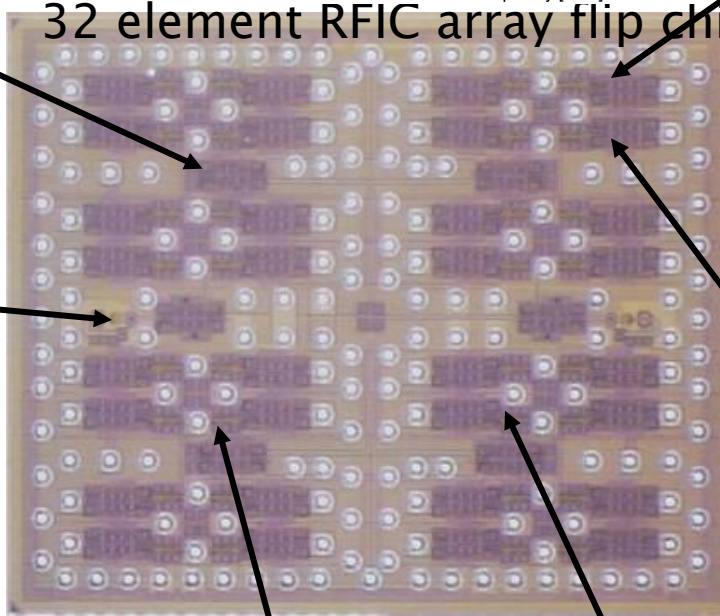
Combiner



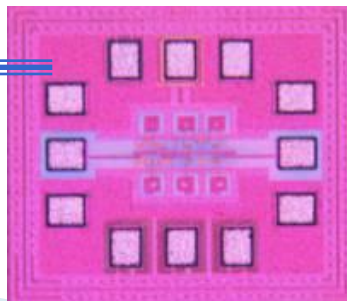
Mixer + LO drive



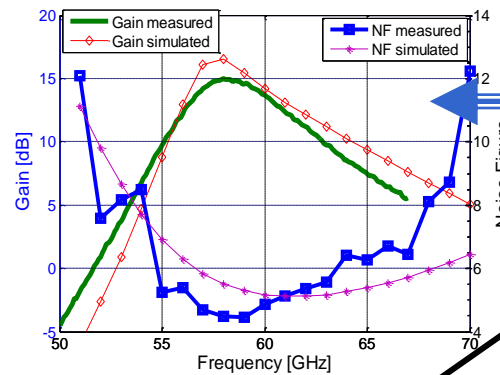
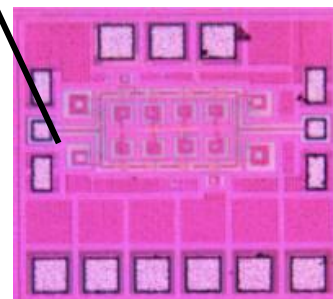
32 element RFIC array flip chip



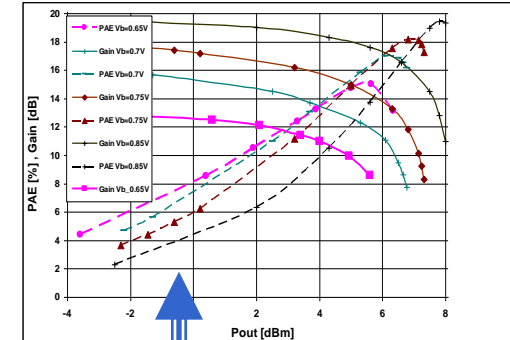
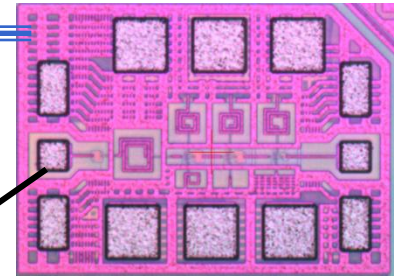
Phase shifter



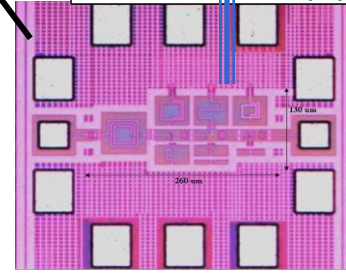
LNA with PA and Switch



LNA

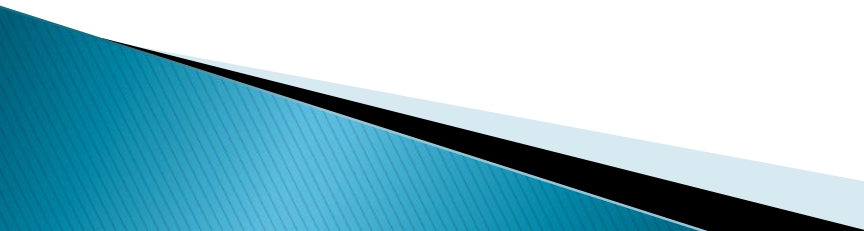


PA





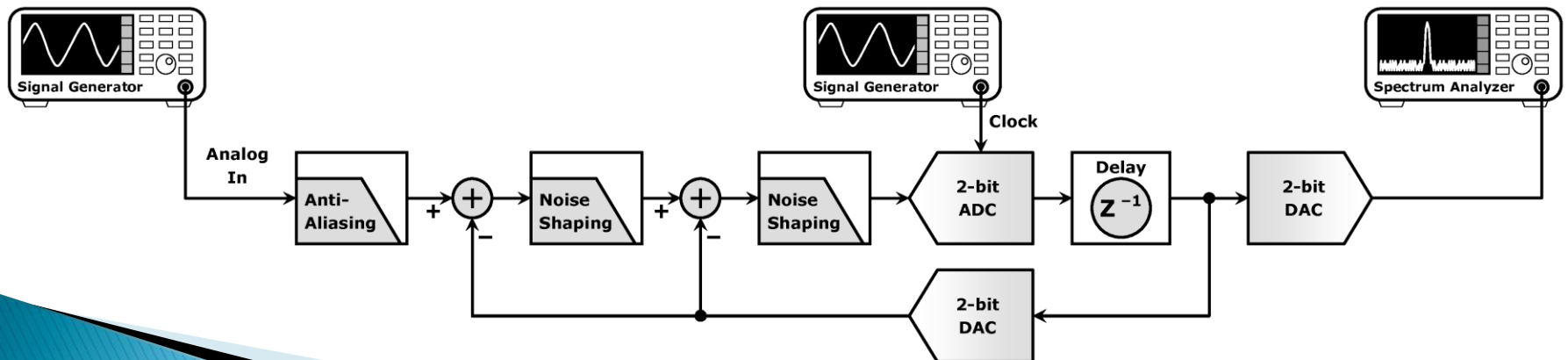
# Next steps

- ▶ Focus on fundamental design issues of the circuits and the full system – based on array data
  - ▶ System level mismatch impact
  - ▶ Element coupling in array
  - ▶ Circuit level limitations: passive switching and amplifier gain boosting vs. bandwidth
  - ▶ Integration of antenna for phase array inside the silicon, and create a very compact system
- 

# Building Blocks for High Speed $\Delta\Sigma$ ADC in InP HBT Technology

Shraga Kraus, Supervised by Dan Ritter

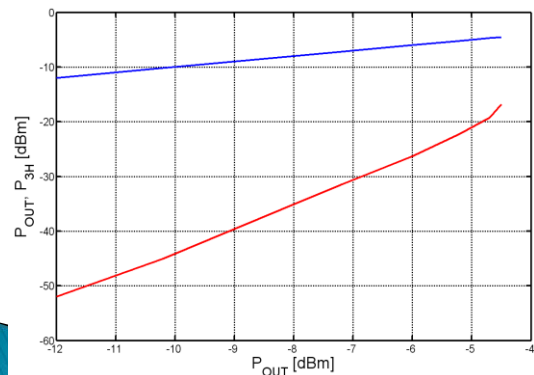
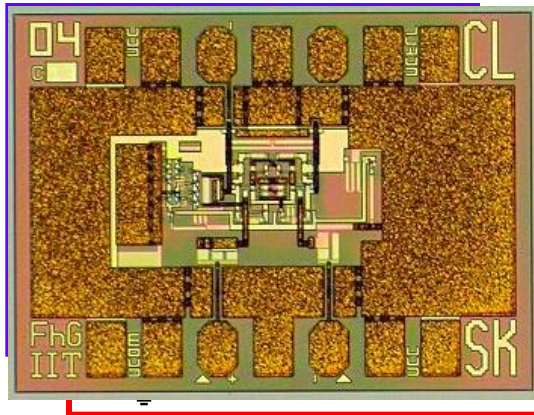
- ▶ Goal: develop analog circuit technology to enable multi-bit  $\Delta\Sigma$  ADC in HBT
- ▶ Stage 1: Building blocks
- ▶ Stage 2: Complete ADC



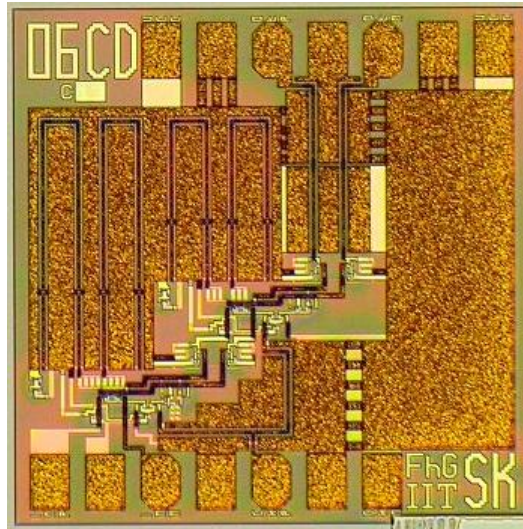
# Summary

▶ Building blocks:

▶ High-gain op amp:

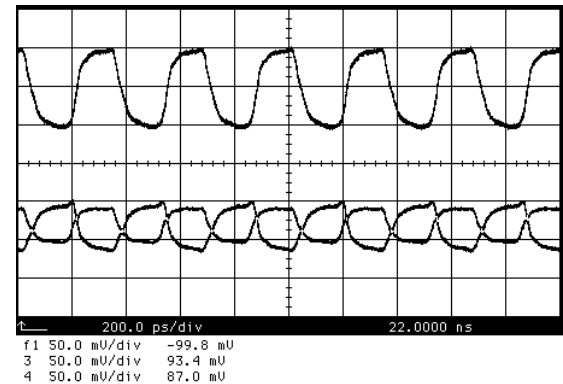
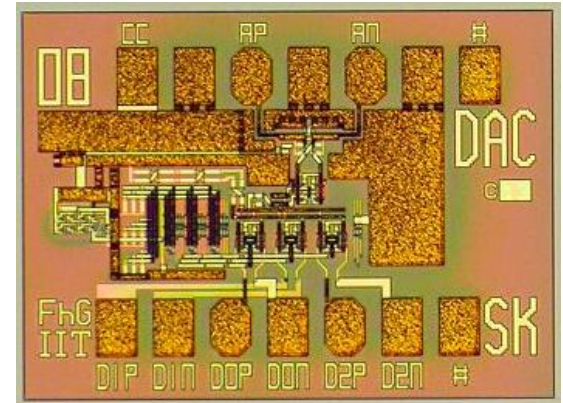


▶ Latched comparator:



Sensitivity (@20 GHz) improves:  
17 mV → 10 mV

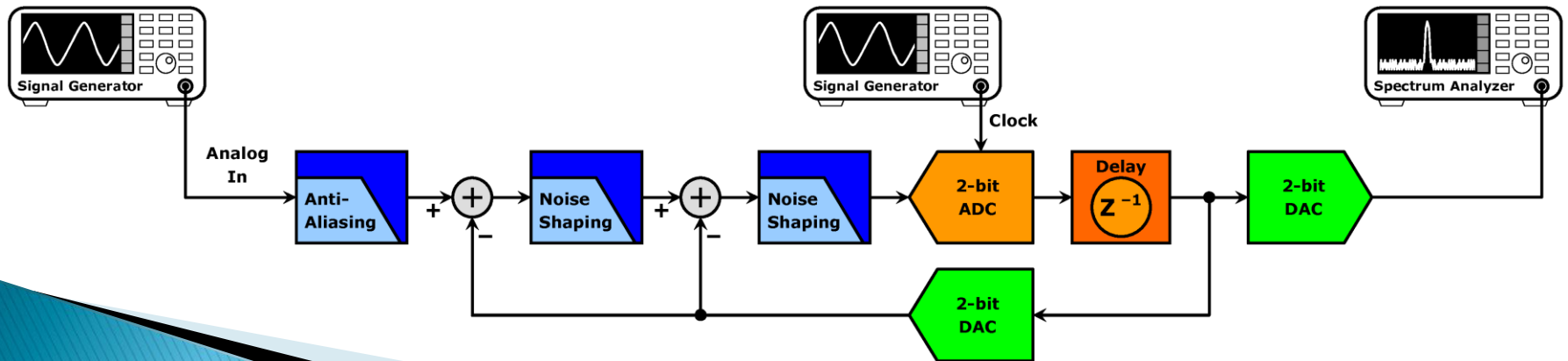
▶ 2-bit DAC:



# Summary

- ▶ Building blocks:
  - ▶ High-gain op amp
  - ▶ Latched comparator
  - ▶ 2-bit DAC

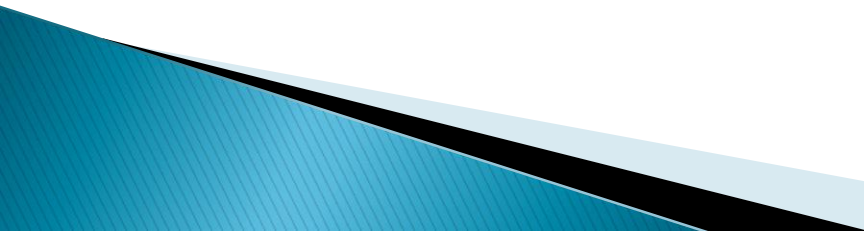
- ▶ Complete ADC



A dark, arched stone tunnel with a metal gate partially open, leading to a bright light. The tunnel is constructed of rough-hewn stone blocks. The gate is made of dark metal bars and is swung open to the left. The light from the opening is very bright, creating a strong contrast with the dark interior of the tunnel. The floor is made of stone and appears slightly wet or reflective.

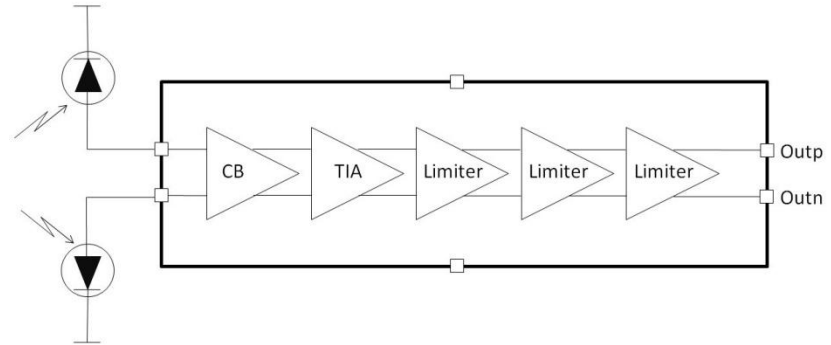
The  
End

# A 40Gbs differential TIA using InP HBT Technology, Eli Bloch and Prof. Dan Ritter

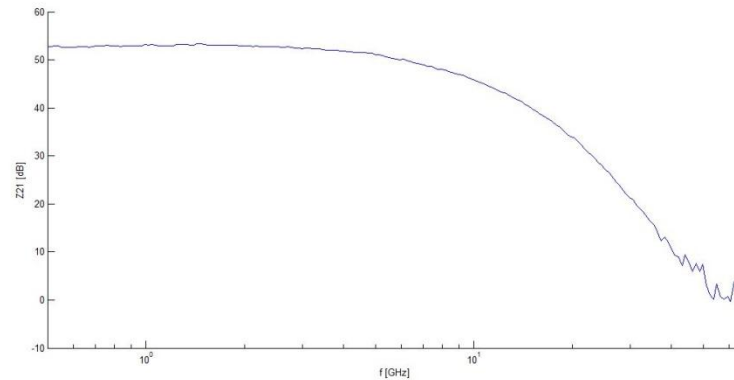
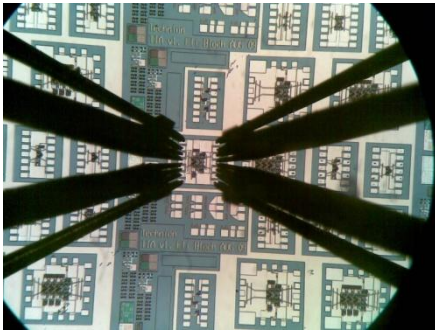
- ▶ 40GHz BW
  - ▶ 2K $\Omega$  Transimpedance gain
  - ▶ Large and small signal combination
  - ▶ High input dynamic range
  - ▶ Output limiting
  - ▶ Low BER
  - ▶ Single device modeling, process optimization and measurements.
- 

# A 40Gbs differential TIA using InP HBT Technology

## ▶ Building Blocks



## ▶ Results:



# Macro Models for Power at RT Level

Anna Kouslik

under supervision of Assoc. Prof. Avinoam Kolodny

- ▶ **Goal:** provide accurate schematic–annotated model for power estimation at RTL allowing
  - Fast feedback to RTL designer on incremental changes
  - Running long and numerous workloads for uArch/RTL analysis
- ▶ **Challenges:**
  - Generating *generic* model working for all type of circuits
    - Most of academia research focused on combinatorial circuits
  - Generating *physical* model
    - Which can be used for what–if analysis for incremental RTL changes

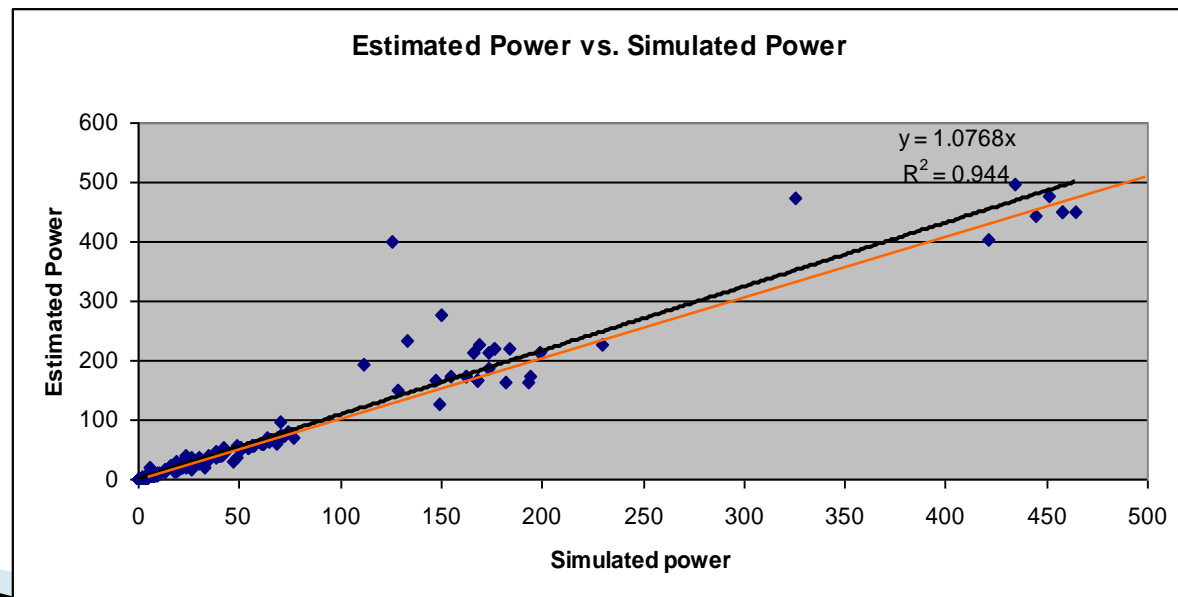


# Macro Models for Power at RT Level

- ▶ Statistical approach based on ‘mapping for power’
  - For each RTL signal identify sub-circuit it is responsible for
  - Assign effective capacitance to each RTL signal derived from its respective sub-circuit
  - Estimate power at RTL by:

$$P_{dyn} = 0.5V^2 f \sum_{\text{all RTL nodes } r} C_r^{eff} \cdot \alpha_r$$

- ▶ Accuracy results on 400 tests:



# Finding the Energy Efficient Curve:

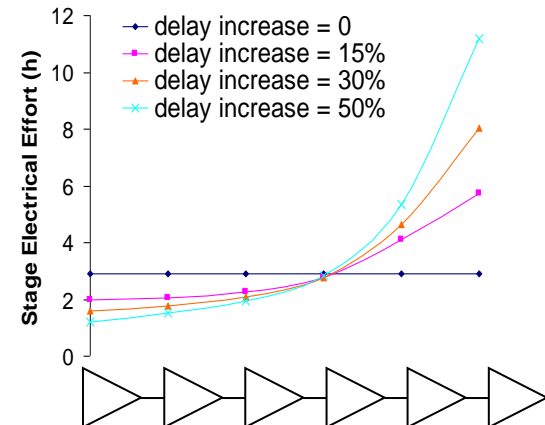
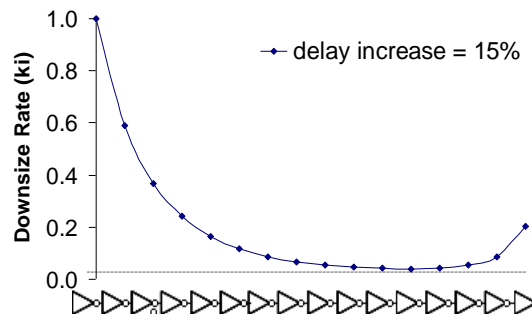
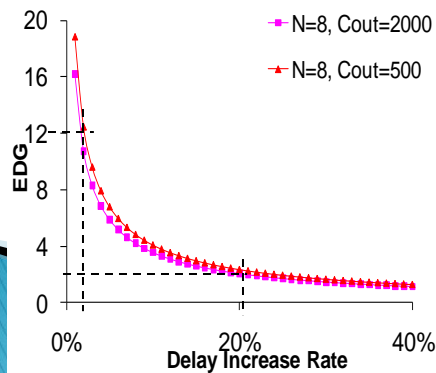
## Gate Sizing for Minimum Power under Delay Constraints

Yoni Aizik and Avinoam Kolodny

- ▶ Main challenge: reduce switching power of a CMOS design in an optimal way, by gate resizing.
  - How to downsize the gates, to gain maximum power savings, and minimum affect on timing?
  - Answer the questions:
    - How much energy can be saved by slowing down the circuit by x percent?
    - How to determine gate sizes for optimal power under a given delay constraint?
    - How to downsize the gates, to gain maximum power savings, and minimum affect on timing? Uniformly?

# Solution

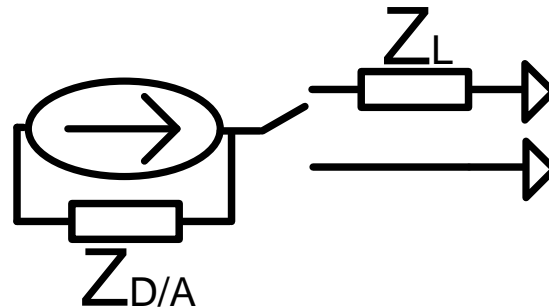
- ▶ Build logical effort model of the circuit
- ▶ Solve the (convex) optimization problem:
  - For a given circuit, with initial sizing, AF, and required performance degradation, find new sizing that maximizes energy reduction.
- ▶ We wrote a tool written over Matlab that solves the optimization problem for a given circuit



# Low Power D/A Converter Design Considerations – Y.Cohen A.Unikovski

- ▶ Current steering D/A converter
  - Single ended operation – poor power efficiency
  - Dynamic range is limited by load and output impedance ratio

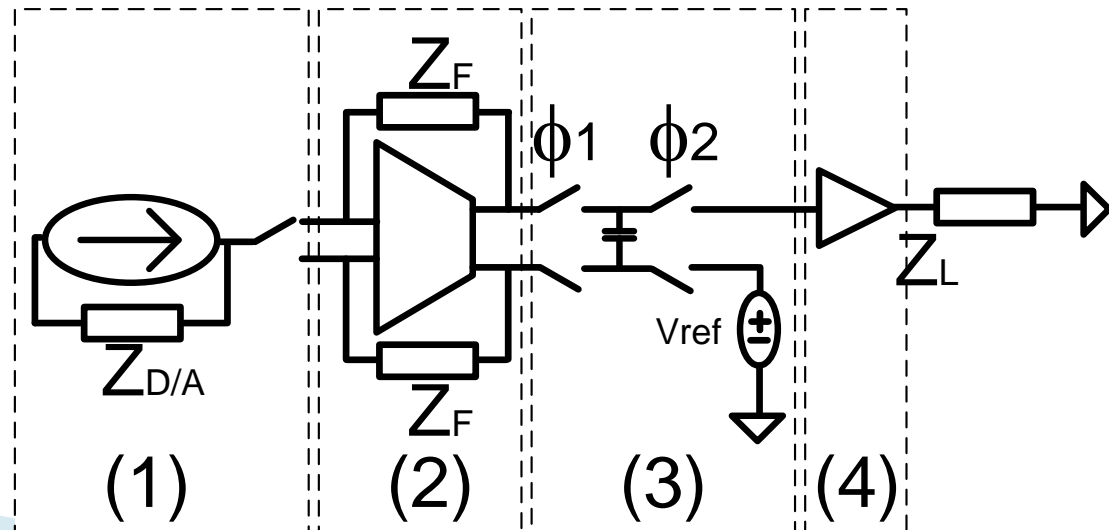
$$Z_{D/A}/Z_L \uparrow \rightarrow DR \uparrow$$



- ▶ The Goal of this research is to improve the power efficiency of the D/A conversion system

# Low Power D/A Converter Design Considerations

- ▶ This work
  - Low power Differential output D/A converter – 0.2mA full scale current (1)
  - Trans-impedance amplifier as the D/A load – improve dynamic range (2)
  - Differential to single ended conversion using switch capacitor architecture (3)
  - Output buffer with impedance matching (4)

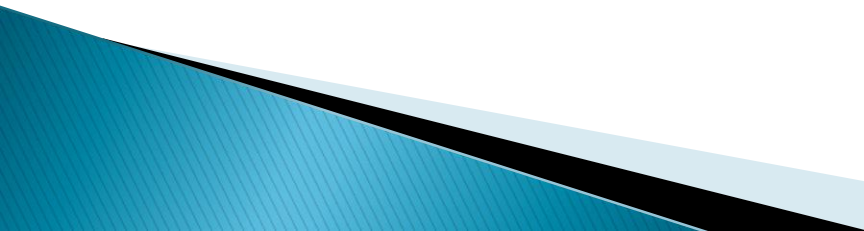


# On-die Power Network Optimization

Michael Sotman (supervisors: E. Friedman, A. Kolodny)

- ▶ Goal: provide recommendations for on-die power delivery network optimization
- ▶ Challenges:
  - Wide current consumption spectrum
  - Multiple voltage domains
  - Lack of on-die decoupling
  - Effective interaction with package
  - Adaptation of power network for on-die power gating and/or on-die voltage regulator

# On-die Power Network Optimization

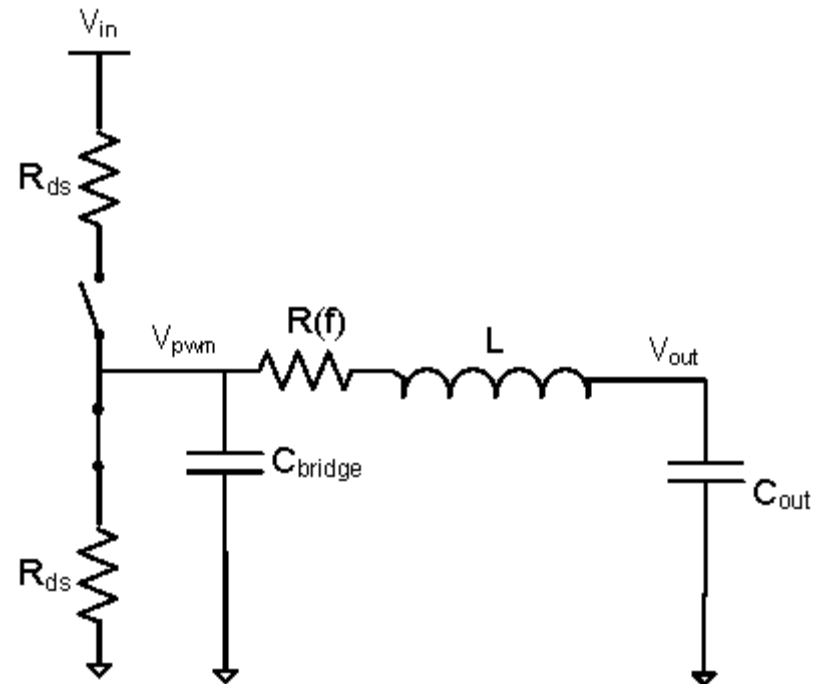
- ▶ Approach: analysis in frequency domain as well as in time domain
  - ▶ Results: TBD
  - ▶ Research program for 2010:
    - Development of idea of parallel routing in adjacent metal layers
    - Analysis of C4 bump effective radius
    - Analysis of recharge influence of on-die decoupling effectiveness
- 

# On-chip DC-DC buck converter

Presenter: Gregory Sizikov

Advisors: E. Friedman, Avinoam Kolodny, Michael Zelikson

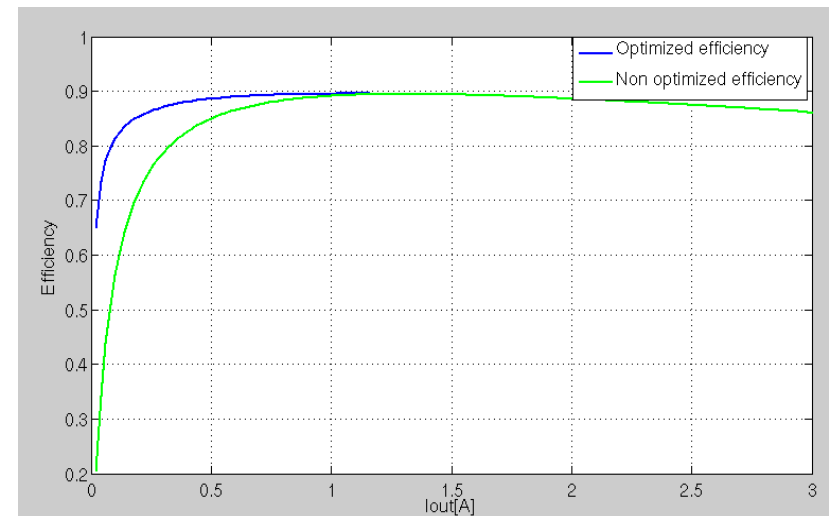
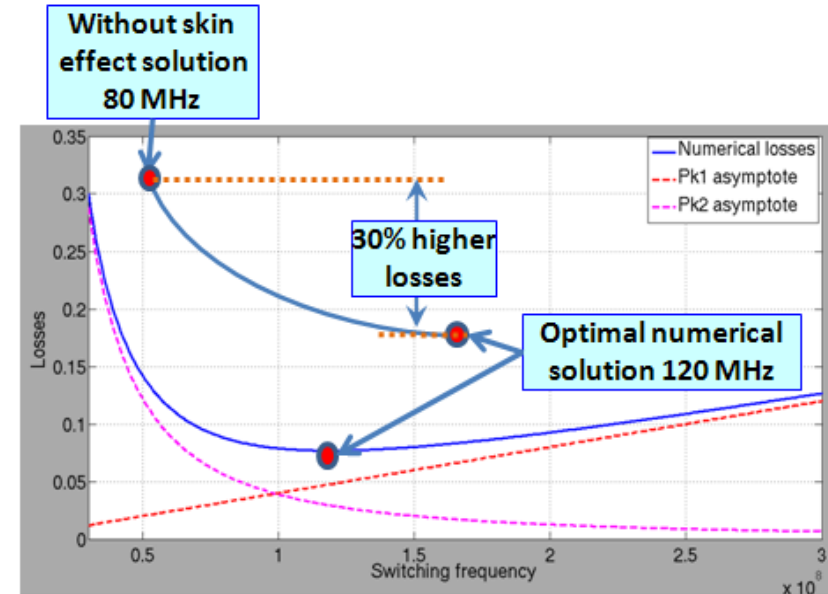
- ▶ The goal of the research is to discuss performance aspects of DC-DC switching buck converter integration
- ▶ Integration challenges:
  - Smaller power path components (LC filter)
  - High switching frequency
  - Sub um process design





# On-chip DC-DC buck converter

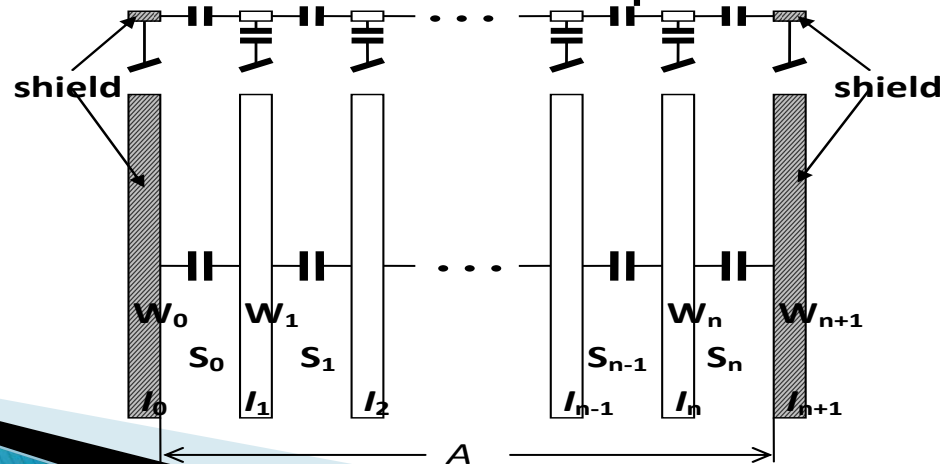
- ▶ The approach taken:
    - Develop analytic expressions for integrated DC-DC converter efficiency, extract their parameters, and validate vs full circuit simulation
  - ▶ Results:
    - Optimal switching frequency found
    - Light load optimization performed
  - ▶ Research program for 2010
    - Expand the optimization to high load current dynamic range
- Publish the results



# Interconnect power optimization under gridded design rules (1)

Konstantin Moiseev (supervisors: S. Wimer, A. Kolodny)

- ▶ Interconnect power is important component of total dynamic power (~50%)
- ▶ The lithography used for 32 nanometers and smaller VLSI process technologies restricts the admissible interconnect widths and spaces to a small set of discrete values
- ▶ The idea: represent size allocation of wires in interconnect channel as a sequential decision problem



# Interconnect power optimization under gridded design rules (2)

- ▶ The problem was shown to be NP-complete
- ▶ DP programming algorithm solving the problem has been developed and implemented
  - The algorithm can handle various combinations of power and delay (i.e. sum power – sum delay, sum power – max delay etc.)
- ▶ Pareto (non-redundant) power–delay curve is generated as a result of algorithm work
  - The designer can choose desired solution according to given power (delay) envelope
- ▶ We showed that that 5 values of available wire widths and spaces are enough to get to as close as 5% from the exact continuous solution and that using just two or three values of widths and spaces is insufficient
- ▶ The application of the algorithm on real design blocks showed reduction of 18% in interconnect power and 9% in interconnect delay on average

