Integration Potential of Active Power Delivery Networks

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Power Delivery Crisis

- Contradictive requirements from platform power management
 - Support huge power dissipation 45 W is a typical figure
 - Enable long (24 hours?!) battery time and fast response time
- Increased functionality in smaller dimensions
 - Higher integration level & higher power density
- Unfavorable (for power delivery) technology scaling trends
- > Voltage regulators are $\leq 60\%$ of a board area
- Power supply pins may limit package shrink

Equivalent scheme



Current flow in different frequency ranges



Major Power Losses reasons

- Voltage Regulator (VR) and AC brick losses
 - Switching losses
 - Inductors losses
- Joule losses on-die, package & socket and motherboard (MB) interconnect.
- > Overvoltage via leakage and excessive active power
 - Leakage loss can be higher than active power consumption
 - Functional when not needed
 - Because of guard bands (GB)

Solution directions

- Smart power management architecture
 - Different power states, allowing tighter voltage control
 - Burst operation when possible, i.e. sleep most of the time
- Active power delivery network
 - Dynamically configurable components
 - Enabling GB reduction
- Selective integration of on-board VRs
 - Consolidation of VRs, MB resources devoted to power supplies
 - Balancing on-board and in-package power dissipation
 - Advanced control approaches

On-die losses reduction

- > Dynamically controlled embedded power gates or sleep transistors. p- or nMOS connected in series to core logic.
 - Saves leakage power
 - May be turned on or off, depending on the logic power state
 - Supports retention voltage, when no activity (toggling)
- > Interesting research direction:
 - Very low drop-out linear regulator. Enables active power savings through GB reduction.
 - Required features:
 - Very high controllable BW (of order of ~500 MHz)
 - Distributed, variable load. Supports [3A, 25A]
 - Drop-out between ~30 mV to 400 mV

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Integrated VRs – board vs. die loss balance



If IVR's efficiency is high enough, platform level efficiency is higher Low package/socket power pin count Mother board area savings

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Integrated Vs should ...

- > High efficiency (>85% over whole current range)
 - Isn't a burden in light load conditions
- Performance similar to that of EVR
- Low cost adder compatible with existing process tech
- Neutral to process technology scaling
- "Friendly" to logic in the neighborhood
 - Low load injection

Consider Switch Capacitor Design



- Capacitance decreases linearly with process scaling
 - Inductance decreases quadratically
- No EMI, low noise injection
- Need smart design/novel architecture to get sufficient η over ~0.4 V range
- Need ~10 µF on-die technology is ready but not available

Summary

- If we do nothing, power delivery will be the limiting factor in the development of integrated systems.
- > On-die active PDN, i.e. local, dynamic power gating, makes significant contribution system power savings
 - Very low dropout linear regulators can be more efficient, but their design is very challenging
- Integration of VR may help realizing multi-power plane designs, but need to be taken with "a grain of salt"
 - If implemented to early makes more harm, than good
 - Switch cap VR seems potentially more "integration friendly" than buck convertor

THANK YOU

– מאגד אלפא - סמינר שנתי אשכולי התקנים ושונות. מגדל העמק 2009

BACKUP

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Voltage budget - breakdown



From voltage regulator to silicon



Energy Efficiency Regulation

Regulation explodes – EU leading

