

ACRC Seminar

Monday, 13 November
11:30-12:30 1003, Meyer Building
Viterbi Faculty of Engineering

Robust Computing Systems: From Today to the N3XT 1,000X



Subhasish Mitra
Stanford University

Abstract

The future of computing systems faces a crisis due to three major challenges:

- **Complexity:** Existing validation and test methods barely cope with today's complexity. New techniques are essential to minimize design flaws (bugs) moving forward.
- **Reliability:** For silicon technologies with remarkably small geometries, several reliability failure mechanisms, largely benign in the past, are becoming visible at the system level.
- **Performance:** Energy efficiency benefits of silicon scaling have plateaued (power wall). Coming generations of abundant-data applications (e.g., deep learning) are increasingly dominated by the time and energy required to transfer data between computing engines and off-chip memory (memory wall).

This talk addresses the complexity and performance challenges:

- **QED** (Quick Error Detection) and Symbolic QED techniques dramatically improve pre-silicon verification and post-silicon validation of digital systems. For billion transistor-scale designs, you can now detect and localize difficult bugs automatically in only a few (~3-8) hours. In contrast, existing approaches might take weeks (or months) of manual work with limited success for difficult bugs.
- **N3XT** (Nano-Engineered Computing Systems Technology) nanosystems leverage unique properties of emerging nanotechnologies to create new computing system architectures that overcome the memory wall and the power wall. N3XT architectures promise to deliver three orders of magnitude energy efficiency improvements for abundant-data applications. N3XT hardware prototypes represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual nanosystems.

Bio

Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University, where he directs the Stanford Robust Systems Group and co-leads the Computation focus area of the Stanford SystemX Alliance. He is also a faculty member of the Stanford Neurosciences Institute. Prof. Mitra holds the Carnot Chair of Excellence in Nanosystems at CEA-LETI in Grenoble, France. Before joining the Stanford faculty, he was a Principal Engineer at Intel Corporation.

Prof. Mitra's research interests range broadly across robust computing, nanosystems, VLSI design, validation, test and electronic design automation, and neurosciences. He, jointly with his students and collaborators, demonstrated the first carbon nanotube computer and the first three-dimensional nanosystem with computation immersed in data storage. These demonstrations received wide-spread recognitions (cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, highlight as "important, scientific breakthrough" by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, National Public Radio, New York Times, Scientific American, Time, Wall Street Journal, Washington Post and numerous others worldwide). His earlier work on X-Compact test compression has been key to cost-effective manufacturing and high-quality testing of almost all electronic systems. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools.

Prof. Mitra's honors include the ACM SIGDA/IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation's Technical Excellence Award, the Intel Achievement Award (Intel's highest corporate honor), and the Presidential Early Career Award for Scientists and Engineers from the White House (the highest United States honor for early-career outstanding scientists and engineers). He and his students published several award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford." Prof. Mitra served on the Defense Advanced Research Projects Agency's (DARPA) Information Science and Technology Board as an invited member. He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).