A 2µW, 0.55V Accurate Low Voltage Power- On- Detector Circuit for IoT Applications

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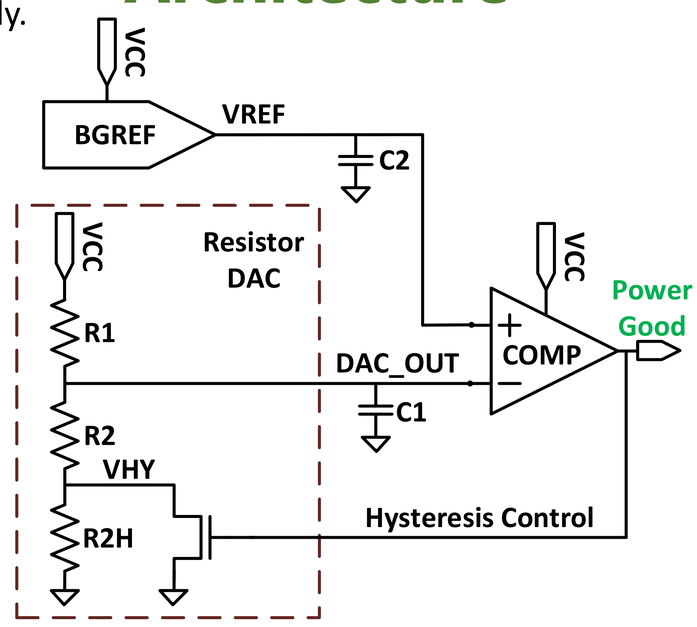
Introduction

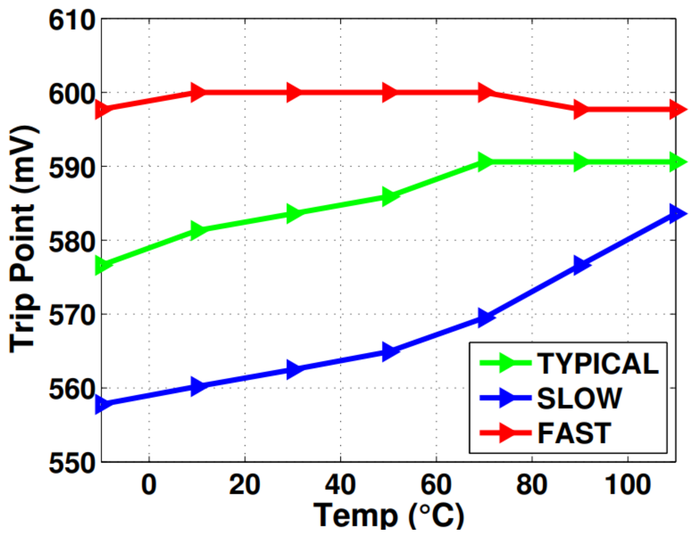
- ✓ Advances in Internet of Things (IoT) applications and the expansion of mobile devices in recent years have made reduced energy consumption and low voltage supply the key feature of analog integrated circuit designs.
- ✓ The POD senses when the voltage supply is stable enough and gives a power-good indication that initiates the reset flow of the SoC.
- ✓ One of the main challenges in designing a POD is that it detects its own supply. In most cases, the internal analog circuits of the POD need to be functional below the nominal supply of the digital SoC circuits.
- ✓ There have been no reports of PODs that can accurately detect voltages lower than 1V from a single supply. This POD circuit can operate accurately at voltages as low as 0.55 V at a nominal power of 2 µW making this POD more appropriate for use in IoT SoCs than previously reported circuits.
- ✓ Some ultra-low-power PODs report ramp-rates solely in the 10 ms - 100 ms range, which indicates that there is a trade-off between the low power operation and the supply ramp-rate that can be accurately detected. Here the pod can detect ramps as fast as 10µs.

Architecture

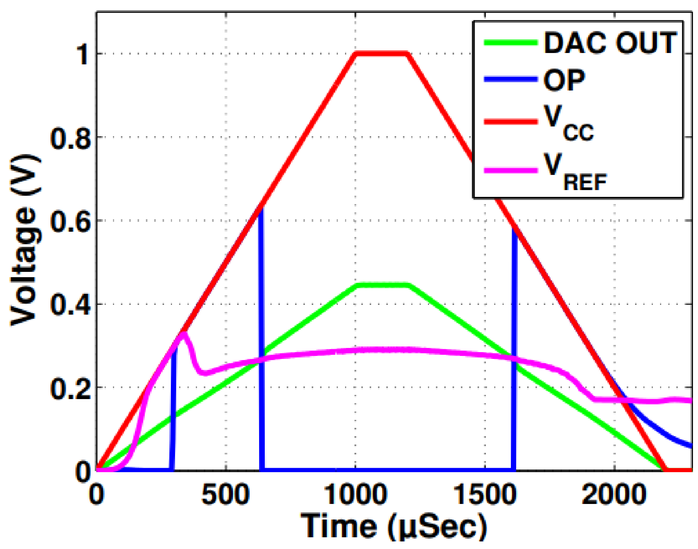


POD Top Level: Suggested POD top level architecture. The input is the supply voltage VCC. When OP de-asserts, this indicates power-good.

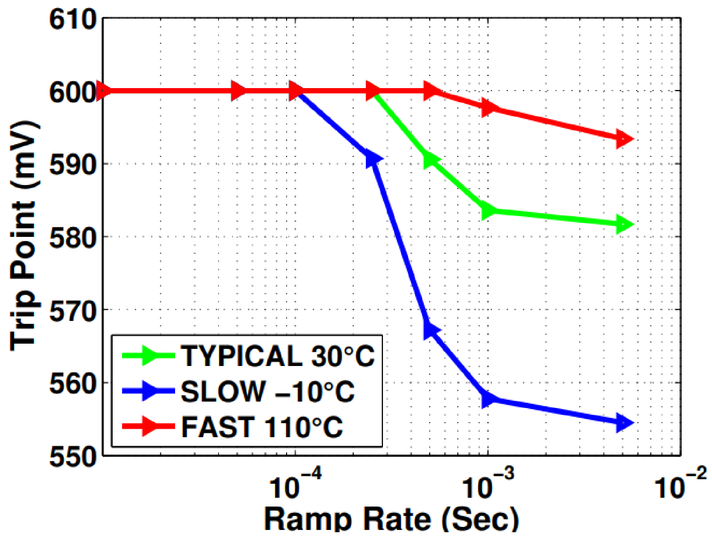
Simulation Results



Trip vs. Temp: POD trip point as function of temperature for a 600mV, supply voltage and a 1ms, supply ramp rate. A maximum PVT variation of <50mV is observed

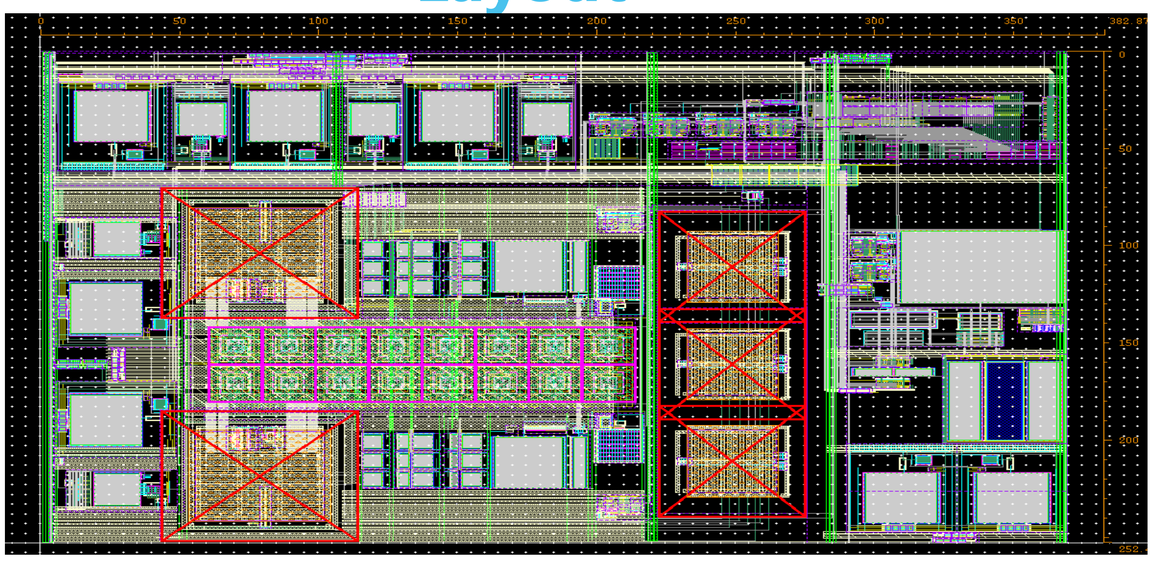


POD Top Level: POD waves for a supply of 1 V and a supply ramp of 1ms. The tip point is configured for 630 mV and a 50 mV hysteresis is observed. When OP is de-asserted this indicates power-good.



Trip vs. Rate: POD trip point vs. ramp rate simulated a 600mV supply configured to trip at 580mV at different process corners.

Layout



POD Layout: The layout of the proposed design in TSMC's 65nm technology

Comparison Table

Reference	11	14	19	20	22	27	This Work
Technology	65nm	14nm	0.18µm	0.13µm	70nm	0.35µm	65nm
Mechanism	BGREF	BGREF	Diode	MOS	BGREF	Diode	BGREF
Nominal Trip Point(V)	0.84	0.8	1.5	0.94	>1.4	>3.9	0.58
Trim Range(V)	NA	0.74-0.91	NA	NA	NA	3.9-5	0.55-0.65
Ramp Rate Range	100µs	50µs	80ms	400ms	50µs	100µs-50ms	10µs-5ms
PVT Variation	80mV	30mV	200mV	200mV	NA	1.3V	< 50mV
Random Variation Sigma	13mV simulated	12mV measured	NA	15mV simulated	25mV measured	NA	2.3mV simulated
Power	4.2µW	496µW	1.5µW	1.5nW	2.4µW	140µW	2µW
Area (mm^2)	NA	0.02	0.012	0.085	0.064	0.029	0.095
Supply Voltage (V)	1	1.1	1.8	1.2	1.4	3.9V	0.55
Temp Coeef (ppm/C)	NA	60	NA	4000	290	NA	140

Comparison Table: Comparison Table of recent reported PODs including this work.

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