2020 Research Day

N-path circuits

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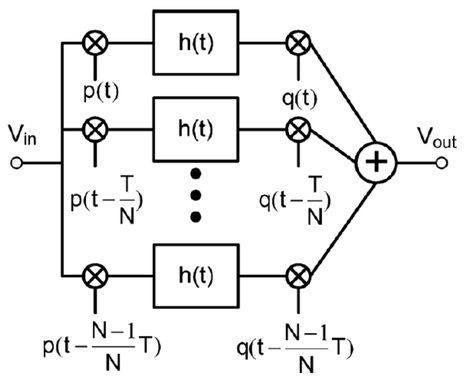
Motivation

Research and implement new circuit topologies, based on N-path circuits, to achieve better performance in 5G and wireless systems.

Introduction

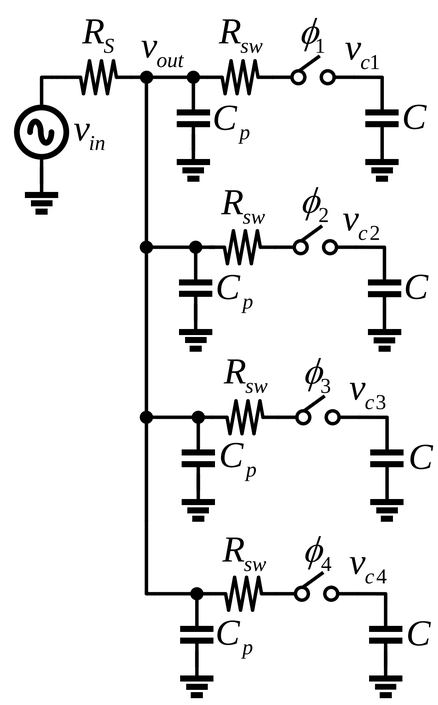
Although known for decades, the N-path topology draws much attention in the past years due to advancement in CMOS process, with the realization of an almost ideal switch.

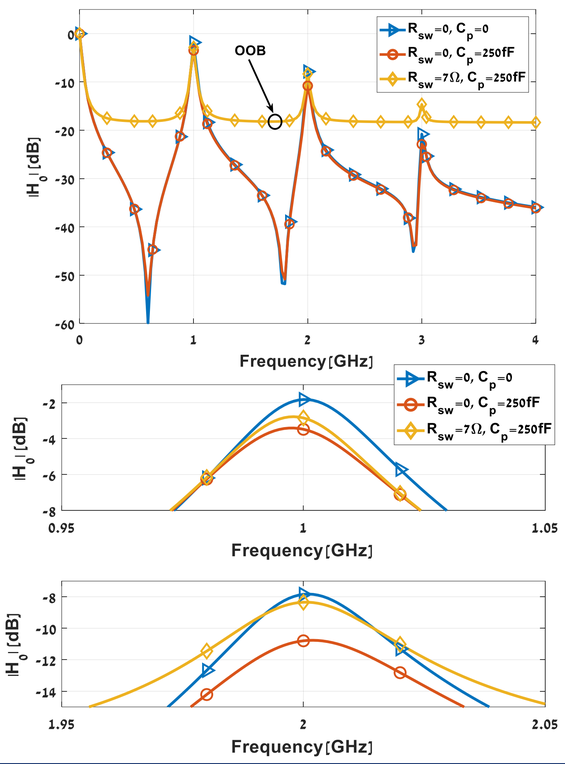


The N-path topology consists of N parallel paths, where each path contains a downconverter mixer, baseband impulse response and an upconverter mixer. All paths are summed at the output. We present three research topics that are related to the N-path topology, with different aspects of implementation, usage and analysis.

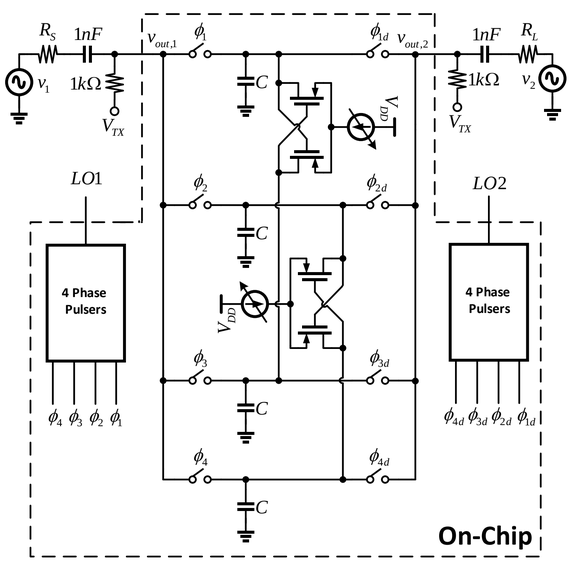
Analysis of The Effect of Switch Resistance and Capacitance On N-path Filters Using State Space Representation

The CMOS switches posses parasitic features, such as ON resistance and shunt capacitance, that cause degradation in insertion loss, noise figure and shift the filter's peak frequencies. We present for the first time a full analytic approach to analyze the switches parasitic effect on the N-path filter performance, using state-space representation.



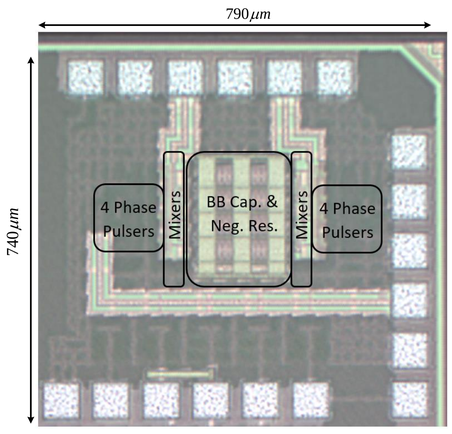


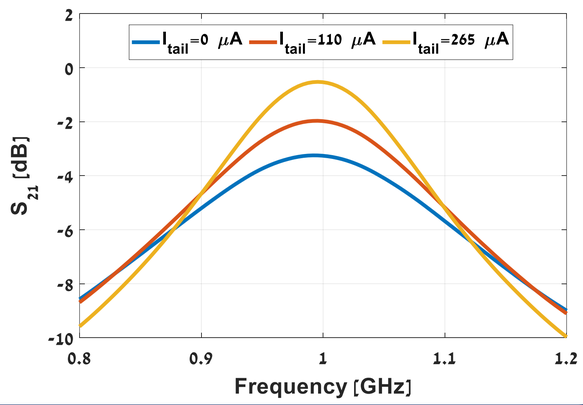
N-Path BPF With Negative Baseband Resistance



2-port N-path band-pass filter with differential negative baseband resistance, to eliminate passband insertion loss.

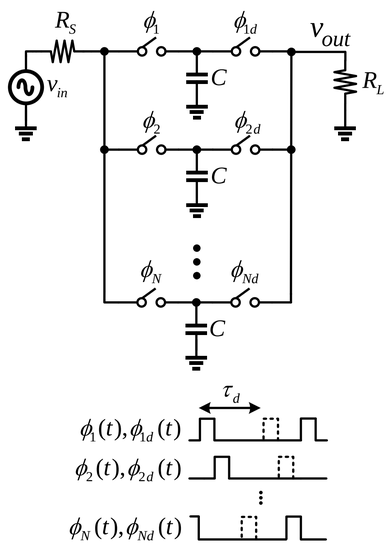
The differential negative resistance was implemented using PMOS cross coupled pair, and the circuit and clocks generators were implemented on a chip, using TSMC 65nm process. Measurement results show elimination of insertion loss for an additional tail current of 265uA at each cross coupled pair.

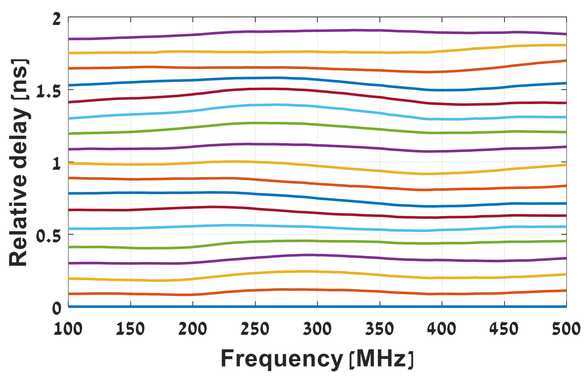


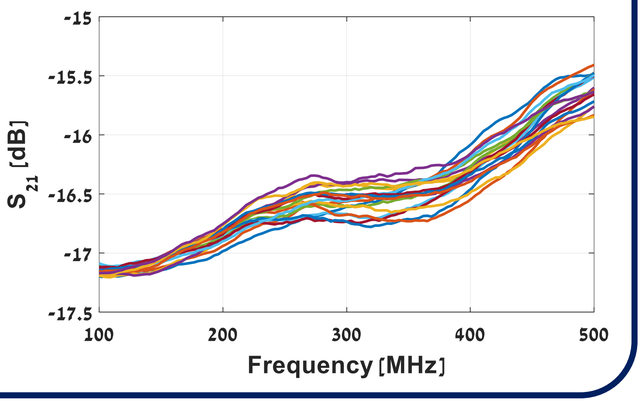


A Low Power Consumption 65-nm CMOS True Time Delay N-path Circuit Achieving 2ps Delay Resolution

A wideband, highly linear, tunable true-time delay circuit, implemented using the N-path two-port filter topology, with relatively low RC constants to allow sampling of input signals instead of averaging it. Measurements of 65-nm chip implementation show up to 2ns delay for bandwidth of 400 MHz, with maximum delay variation over frequency of 22 ps, delay resolution of 2 ps and power consumption of 9.6 mW.







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