2020 Research Day

Spin-Transfer Torque MTJs in Logic and Cache Memory Applications

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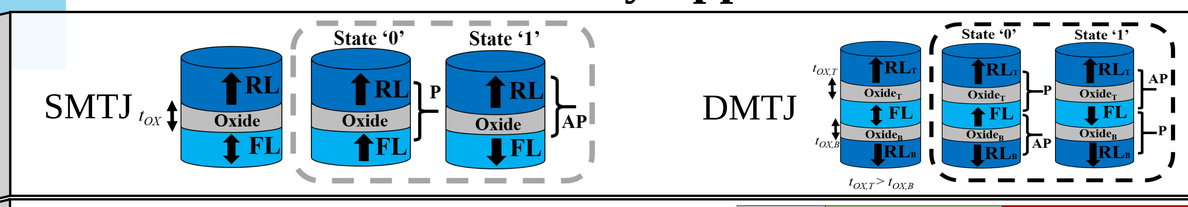
Introduction

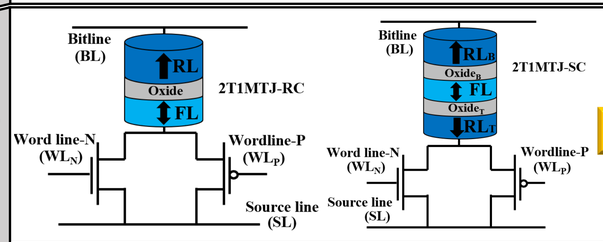
- Spin-transfer torque magnetic RAMs (**STT-MRAMs**) have recently gained keen interest for **non-volatile cache memory applications** thanks to their **potential for low-power and high-speed operation, compatibility with CMOS process, and high integration density.**
- **The technology-scalability** of STT-MRAMs **still remains challenging**, mainly due to the **need to reduce the switching currents** required for information writing.
- The aforementioned challenge can be addressed by using **double-barrier magnetic tunnel junctions** (**DMTJs**) with two reference layers (RLs) **instead of conventional single-barrier MTJs** (**SMTJs**).
- Additionally, STT-MTJ based circuits have shown **attractive potential to design** efficient non-volatile **logic-in-memory (NV-LIM) architectures**, which assure low power and increased speed.

Cache Memory Application: A Device-to-System Level Simulation Framework

Device-Level



Circuit-Level



Results

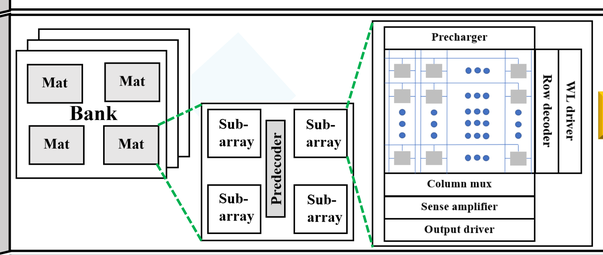
Bitcell type*	Writing op. (WER= 10^{-7})		Reading op. (RDR=10^{-9})		
	t_{write} [ns]	E_{write} [fJ]	I_{read} [µA]	E_{read} [fJ]	V_{SM} [mV]
28-nm node					
SMTJ	3.5	189.5	26.1	9.0	192.1
DMTJ	1.1	48.5	7.2	0.9	79.3
24-nm node					
SMTJ	3.2	138.7	18.7	6.1	189.8
DMTJ	1.0	35.8	5.1	0.6	77.2
20-nm node					
SMTJ	2.9	92.4	11.9	3.5	182.7
DMTJ	0.9	24.3	3.3	0.3	72.0

* 2T1MTJ-RC (231 F^2) for SMTJ and 2T1MTJ-SC (131 F^2) for DMTJ

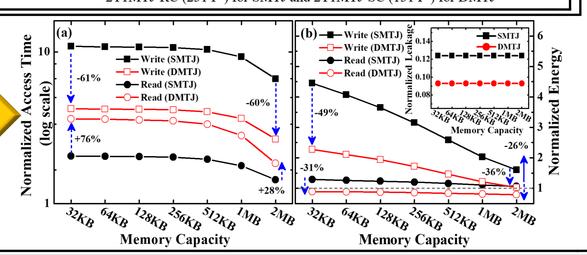
SMTJ-based bitcell vs. DMTJ-based

writing operation: better write speed (more than 3X) and lower write energy (more than 3.8X);
reading operation: lower read energy (-90%), but reduced sensing margins (-60%) due to the lower I_{read} (-72%).

Mem. Arch.-Level



Results



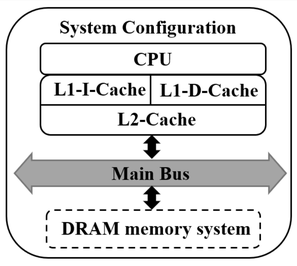
SRAMs vs. STT-MRAMs:

Reduced leakage (-90%) with penalty in terms of write/read access times and write energy consumption.

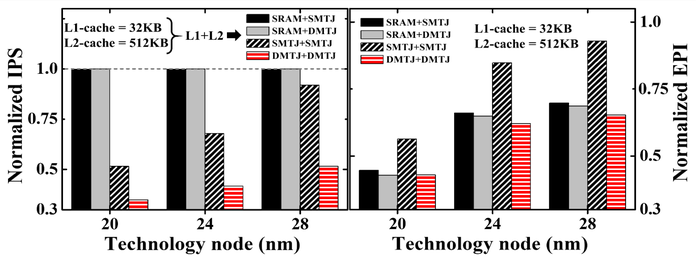
SMTJ- vs. DMTJ-based MRAM:

- ❖faster (+60%) under write access, but slower under read access;
- ❖more energy-efficient in the whole memory capacity range;
- ❖less area hungry (-40%).

System-Level

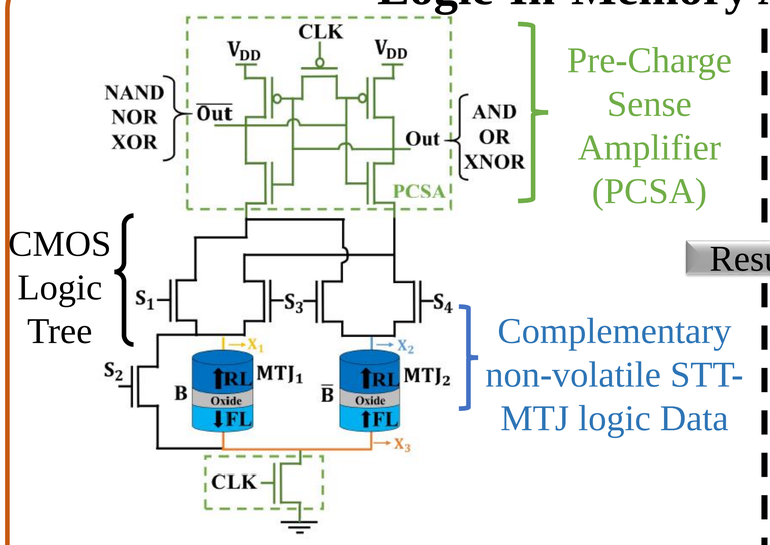


Results



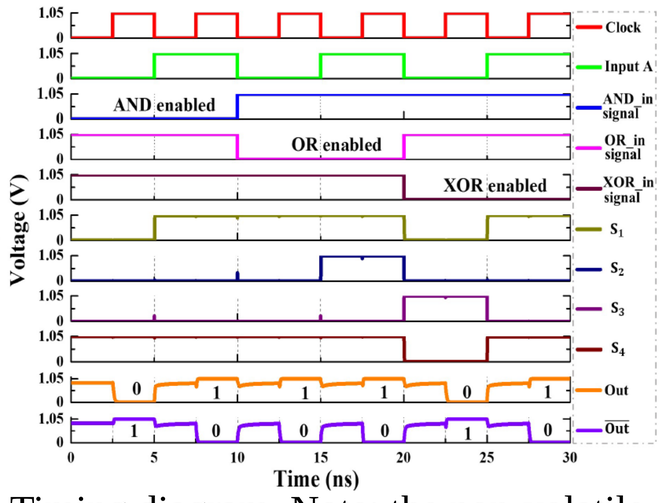
System performance in terms of instructions per second (**IPS**) and cache energy consumption in terms of energy per instructions (**EPI**) averaged on a set of different benchmark applications and normalized to the SRAM+SRAM (L1+L2) cache configuration.
DMTJ-based STT-MRAMs allow achieving the **lowest EPI** at the cost of reduced system-level performance.

Logic-In-Memory Application: Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit



Proposed hybrid CMOS/STT-MTJ circuit.

Results



Timing diagram. Note: the non-volatile logic input is B = '1'

POST-LAYOUT SIMULATION RESULTS FOR THE PROPOSED AND THE STATE-OF-THE-ART HYBRID CMOS/STT-MTJ NV LOGIC CIRCUITS

Design	Operation	Delay (ps)	Energy (fJ)
Proposed circuit	AND/OR/XOR	136.6	8.0
State-of-the-art circuit (2014)	AND	128.3	4.8
State-of-the-art circuit (2018)		113.2	3.9
State-of-the-art circuit (2014)	XOR	127.0	6.2
State-of-the-art circuit (2018)		94.5	4.5
State-of-the-art circuit (2014)	OR	95.2	5.6
State-of-the-art circuit (2018)		91.8	4.6

- The design leads to increase both delay (+29% on average) and energy (+66% on average) due to the larger number of transistors. However, a reconfigurability is offered by the proposed circuit, allowing multiple logic operations by the same architecture.

Conclusions

Cache memory applications

- The use of DMTJs instead of conventional SMTJs in STT-MRAMs cache applications has been investigated through a device-to-system level simulation framework.
- Obtained results prove that DMTJ-based STT-MRAMs are credible candidates for replacing conventional semiconductor-based cache memories for the next-generation of low-power microprocessors with on-chip non-volatility.

Logic in memory applications

- A new hybrid CMOS/STT-MTJ NV logic design is proposed, which allows implementing multiple logic functions (i.e. AND/OR/XOR) within a single circuit architecture.
- Obtained results show that, when compared to state-of-the-art designs, our circuit exhibits a penalty in both delay and energy due to the use of a larger number of transistors. Nevertheless, the operation flexibility offered by the proposed circuit represents a promising feature to reduce area occupancy and design complexity in NV-LIM circuit applications.

These works were(will be) presented in:
1. E. Garzón, *et. al.*, "Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory," *IEEE International Conference on Electronics Circuits and Systems (ICECS)*, Genova, Nov. 29, 2019.
2. E. Garzón, *et. al.*, "Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit for Logic-in-Memory Applications," Accepted and to be presented in: IEEE Latin American Symposium on Circuits and Systems (LASCAS), San José, Costa Rica, 2020.