2020 Research Day

VLSI Delay Tuning by Signal Shielding Measurements and Clock-Tree Application

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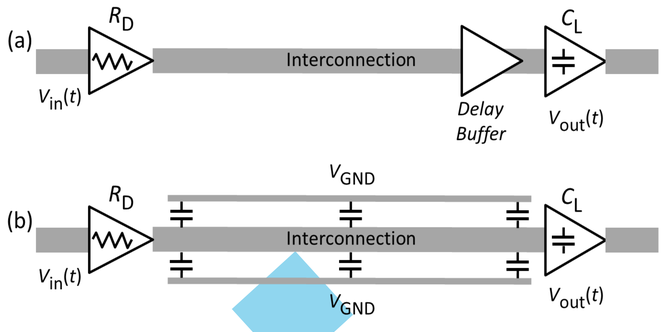
Goal

Reduce the effect of process variation on signal (e.g. clock) propagation delay.

Method

Use wire-shielding space tapering instead of dedicated delay buffers for propagation delay tuning.

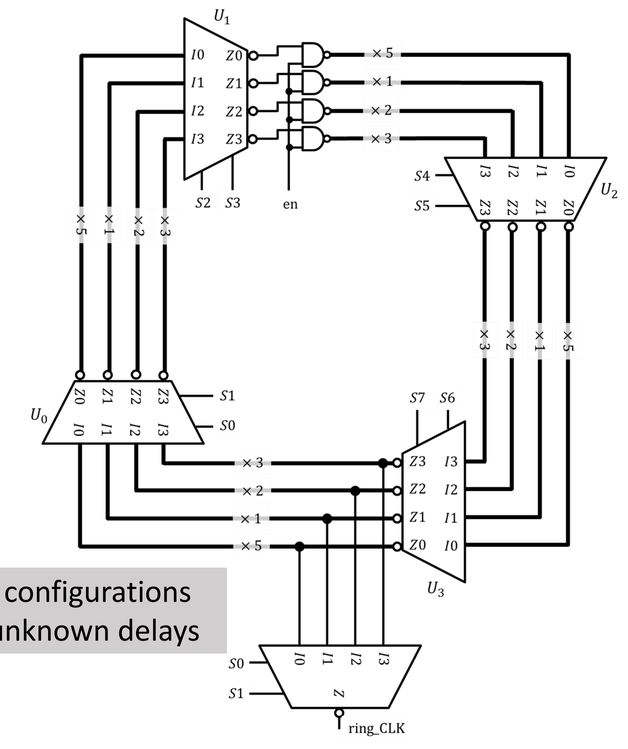
Motivation



Wires (b) are considerably less sensitive to manufacturing process variations than delay buffers (a), which makes the IC design more robust. Results in fewer required layout design changes (due to ECOs).

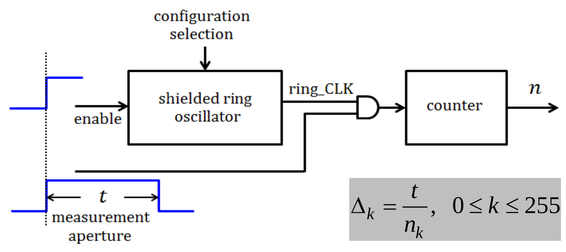
Shield Delay Extraction From Silicon

A test chip was fabricated in TSMC 16nm technology, provided by Marvell. The chip included four shielded ring oscillators, positioned $3880[\mu m]$ apart in height and $930[\mu m]$ in width. Each oscillator employs $1,2,3,5 \times s_{min}$ spacings and $1 \times w_{min}$ wire width.
The post-silicon delay values for the 16 segments were extracted via least mean square (LMS) estimation. Estimation error (compared periods using different same-length paths) is negligible.

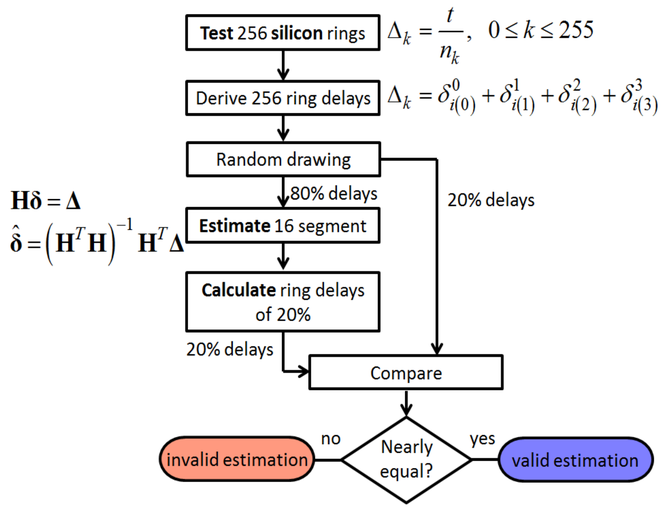


256 configurations
16 unknown delays

Test circuit



Post-silicon Estimation Quality

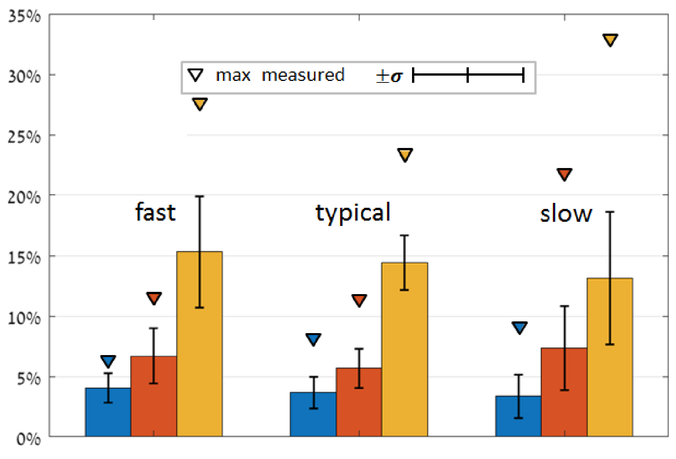


	Typ 0.8v 25°C-105°C	Typ 0.9v 25°C-105°C	Typ 1.0v 25°C-105°C
Err Max[%]	0.07%	0.14%	0.14%
Err Avg[%]	0.02%	0.04%	0.04%
Err StdEv[%]	0.02%	0.03%	0.04%

These results confirmed the validity of the post-silicon estimation methodology.

Post-Silicon Delay Variation

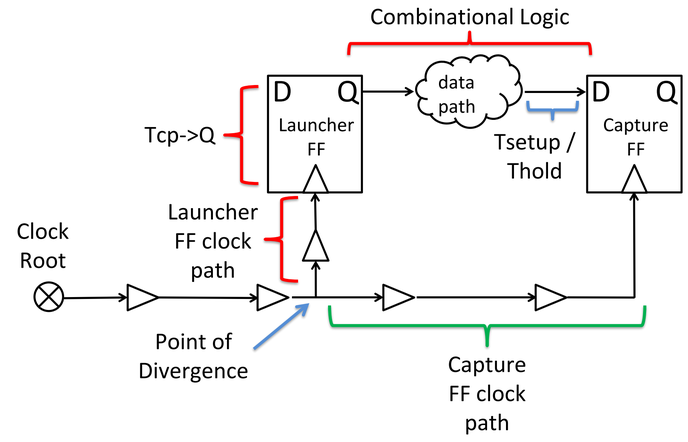
Shielding ☺ Vs. Delay buffer ☹



The delay variation that achieved by shielding is far more stable than the delay variation that obtained by delay buffers.

Useful Skew Delay Insertion

Useful skew technique shifts the arrival time of the sequential elements clock relatively to a nominal clock arrival. The shifts are obtained by inserting delay elements into the clock network.



Shield Delay Clock Tree Application

A DME based clock-tree synthesis that supports shield delay and buffer delay was tested on two of Marvell's designs. The first was ARMv7® based processor that operated at 1.6[GHz]. The second was a memory controller that operated at 800[MHz].

	Buffer Insertion	
	ARM® CPU	Memory Ctrl.
# *FF*s	70K	40K
# *FF*s with useful skew	3892	1215
CTS wire length [mm]	534	305
# delay buffers	8785	4986
# delay buffers in critical path	12	7
Insertion delay [ps]	557	483
Dynamic Power [mW]	4783	1345
Leakage Power [mW]	70.7	19.8

	Shield Delay	
	ARM® CPU	Memory Ctrl.
# FFs	70K	40K
# *FF*s with useful skew	3892	1215
CTS wire length [mm]	837 (x1.56)	480 (x1.57)
# delay buffers	0	0
# delay buffers in critical path	0	0
Insertion delay [ps]	553	483
Dynamic Power [mW]	4623 (-3%)	1300 (-3%)
Leakage Power [mW]	66.8 (-4.5%)	18.8 (-5%)

The two methods represent a trade-off between the number of clock buffers and the clock wire length. Moreover, for the CPU case the shield-delay implementation saved 12 cascaded buffers variation, which is equal to ~13[ps] of delay variation. This can be directly translated to speed (clock period).
Similarly, for the hold constraints, saving those delay buffers translates into relaxed overall variation requirements. Thus, the required number of delay buffers for satisfying hold constraints is greatly reduced.

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