2020 Research Day

Efficient Transmitter Architecture for Millimeter Wave Phased-Arrays

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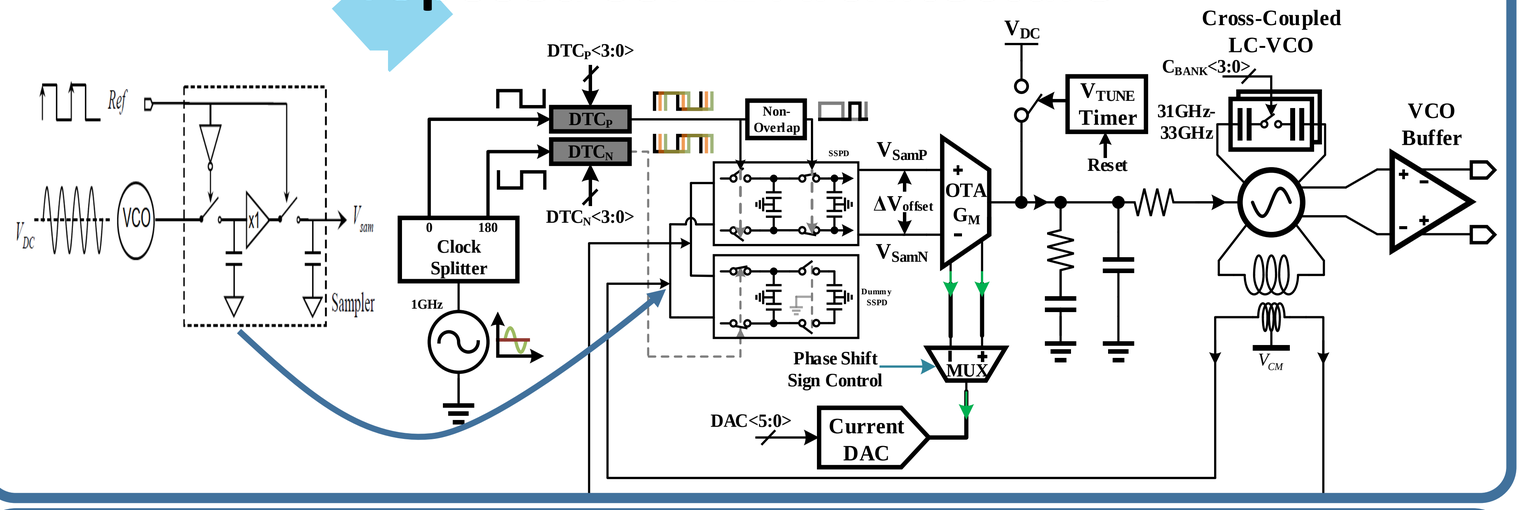
Motivation

This Research focus on very low power PLL solution at mm-wave frequencies for highly scalable integrated phased-arrays working in 5G communication standards

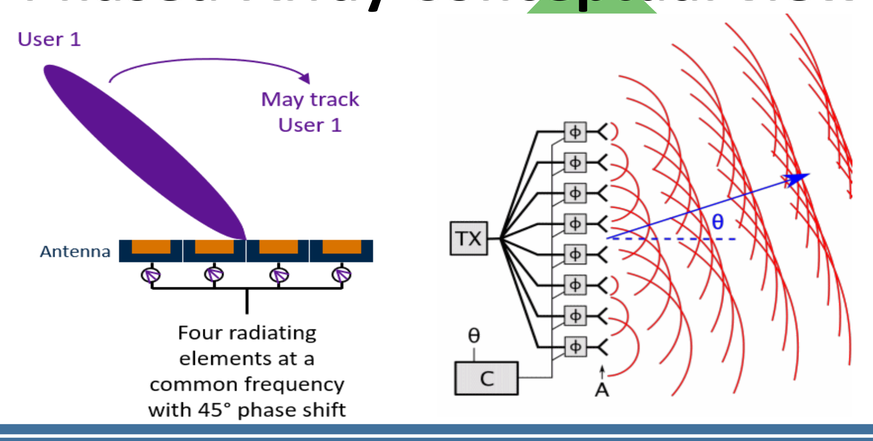
Introduction

- Classical architectures for phased arrays typically include a central local oscillator (LO), high frequency LO distribution network and RF phase shifters in order to achieve antenna beamsteering.
- This architecture requires high power LO driving since high frequency distribution and RF phase shifters draw significant power due to losses at mm wave.
- The proposed topology based on phase-locked loop per element. High frequency distribution is reduced to low frequency reference signal distribution.
- For low power PLL architecture, the divider-less Sub-Sampling PLL (SSPLL) is used.
- RF phase shifters removed, instead high-resolution phase shifting is done in baseband, and part of the PLL design.

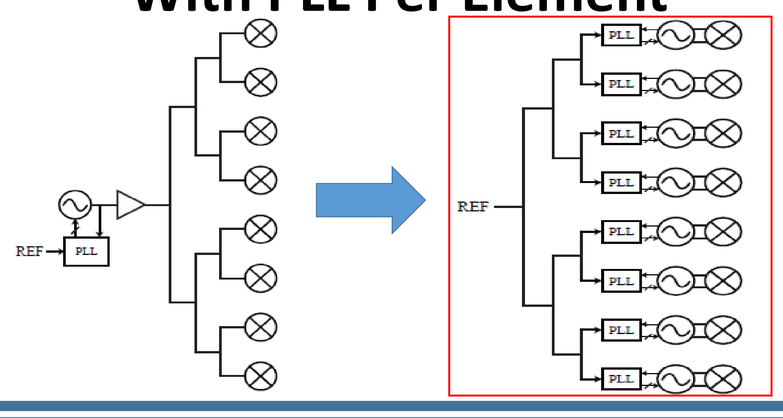
Proposed SSPLL Architecture



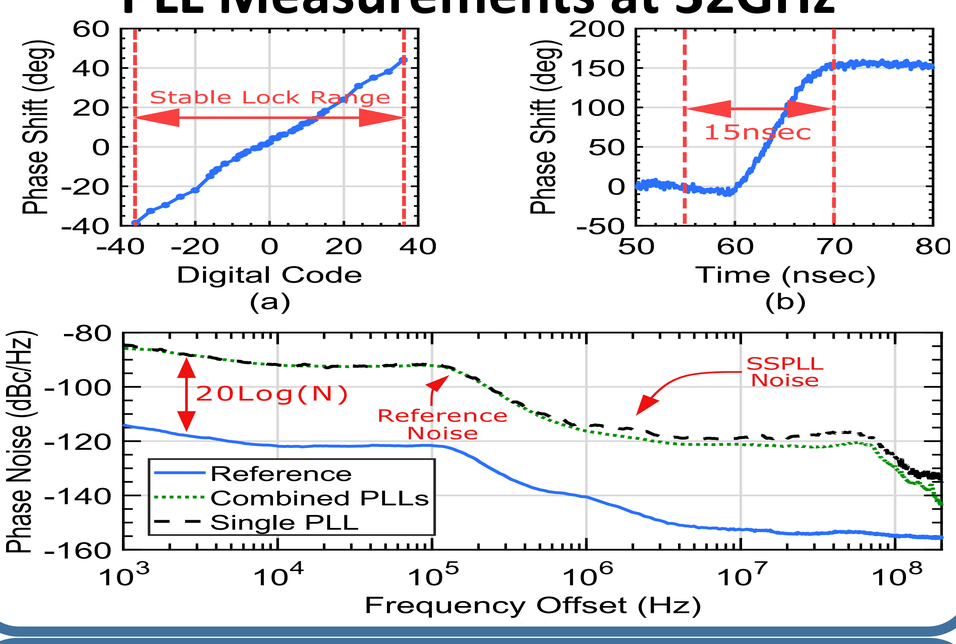
Phased-Array Conceptual view



High to Low Frequency Distribution With PLL Per Element

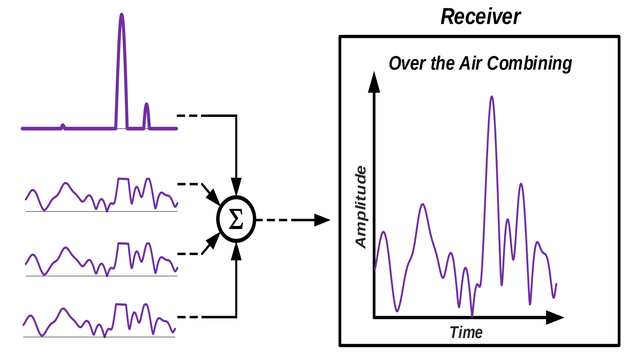


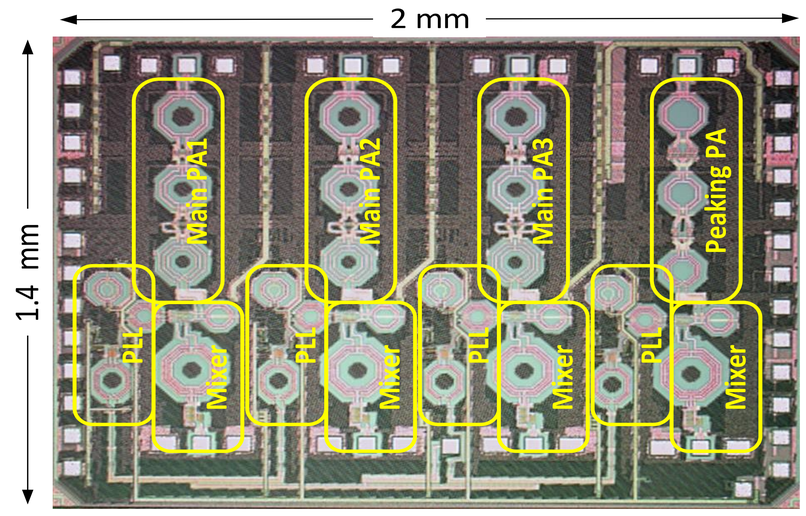
PLL Measurements at 32GHz



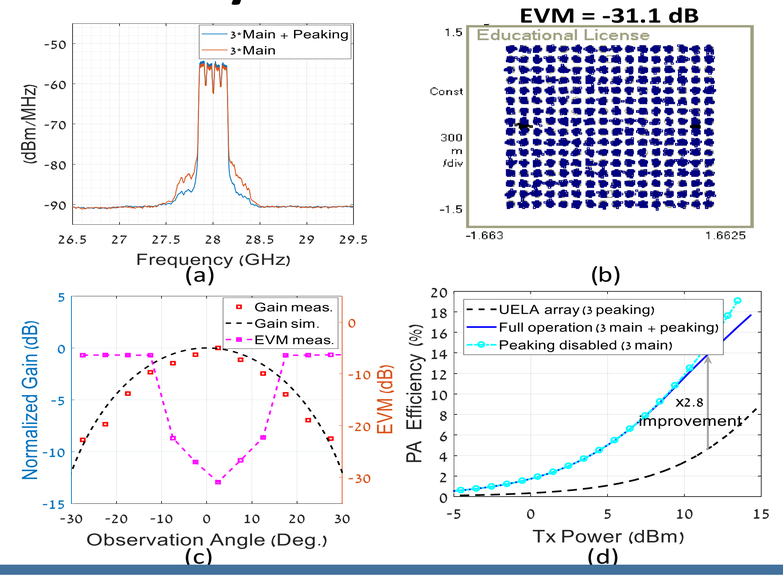
Phased-Array Chip Implementation

A 4-element phased array transmitter was implemented in standard 65nm process.





Phased-Array Measurements at 28GHz



Conclusion

This proposed architecture based on SSPLL with LO phase-shifting achieves 1^0 phase resolution with very low power of 4.2mW and integrated phase noise of 87fs per chain. This topology can easily be scaled to larger arrays requiring only a routing of a 1GHz clock.