Research Day 2020

Process Monitor – Vth, Mobility and Temp. Measurement 65nm TSMC

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Introduction

- ✓ The design margins for mixed signal designs depend significantly on process parameters and their distribution across the wafer and this is especially relevant for mismatch
- ✓ A small monitoring circuit is located on the same die as the host circuit, thus ensuring that the sample provides an accurate representation of the devices on the chip, such monitor cells can be used to obtain the mean and the standard deviation of the most important parameters
- ✓ The data can be accessed on each die at any time during the processing and manufacturing chain, even in the field
- ✓ Mismatch causes threshold voltage variations between nominally identical CMOS transistors
- ✓ The P.M. can be used to calibrate parameter fluctuation models in circuit-level simulations. The P.M. is also a feedback path for fabless companies to ensure Process compliance with the foundry-supplied process design kit (PDK)
- ✓ The extracted data can be utilized to increase or reduce circuit design margins resulting in increased yield and helps to identify critical path

General Key Specifications

- Area of 3000µm^2
- Current consumption of 110µA
- Line sensitivity of 3300ppm/V – 1V-1.5V supply range
- Temp. range of -10°C – 125°C
- Monte-Carlo 1σ < 3.3mV – V_{TH} Device inherent variation
- Digital output using Sigma-Delta ADC + 11-bit ripple counter
- V_{TH} and μC_{ox} sensor in one
- 4 types of transistors – nmos svt/lvt and pmos svt/lvt

Silicon Measurement

- Preliminary results
- Room temperature
- Supply voltage dependence
- 70 samples per measurement
- Averaged measurement to filter noise
- V_{TH} and μC_{ox} measurements

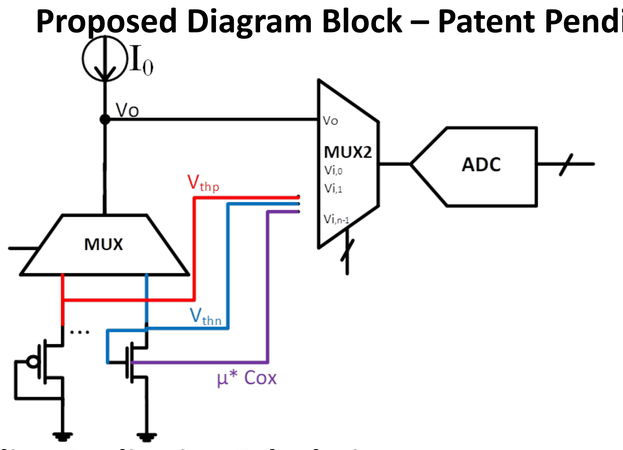
Functional Circuit with SDM Simulations

- Simulation with 10-bit counter
- The relation between the analog input and output is:

$$\frac{V_{in}}{V_{ref}} = \frac{V_{th}}{V_{bg\_ref}} = \frac{counter's\ op}{2^{10}} \rightarrow V_{th} = \frac{counter\ \#\ of\ 1's}{1024} \cdot V_{bg\_ref}$$

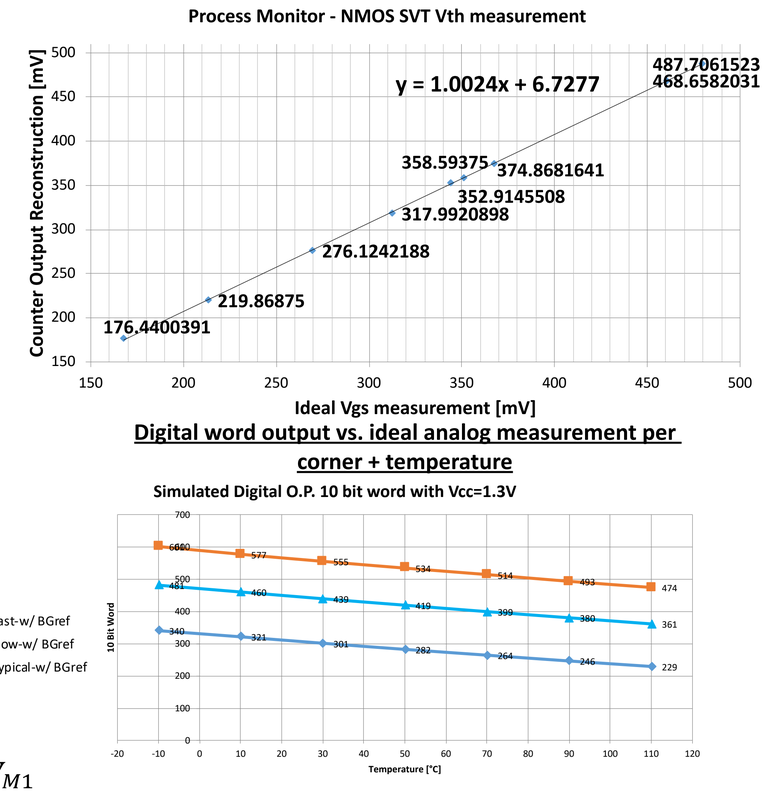
- The above Vth is the reconstructed voltage

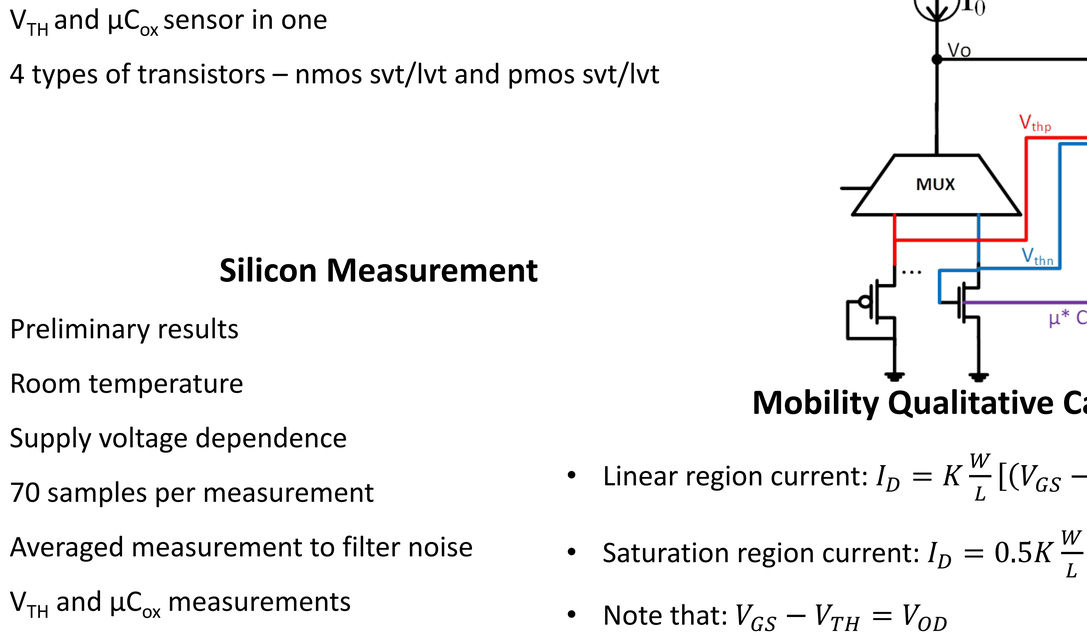
Proposed Diagram Block – Patent Pending



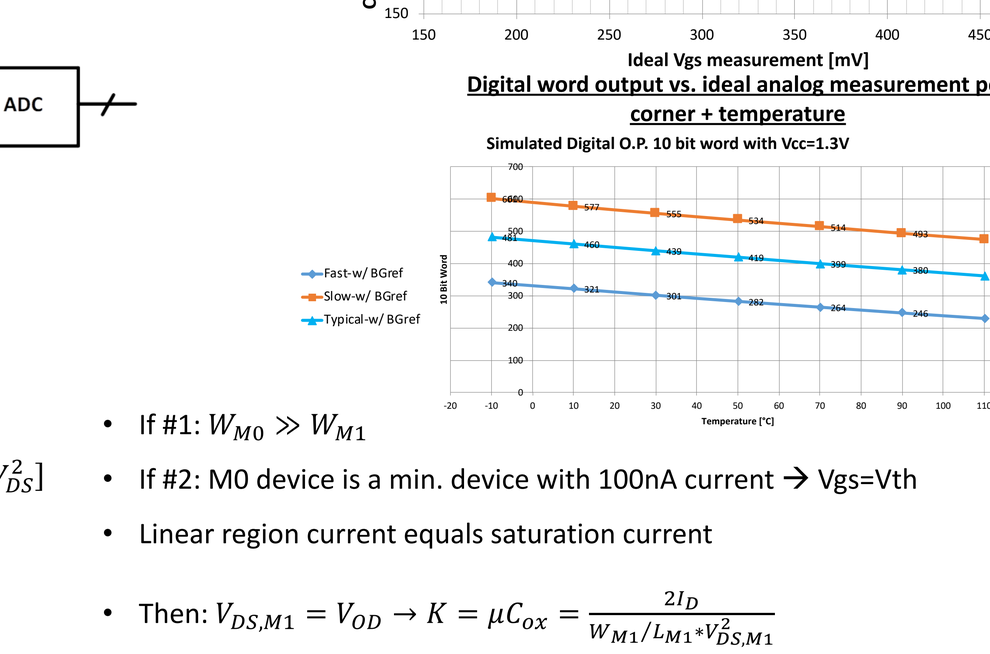
Mobility Qualitative Calculation

- Linear region current: $I_D = K\frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2]$
- Saturation region current: $I_D = 0.5K\frac{W}{L}(V_{GS} - V_{TH})^2$
- Note that: $V_{GS} - V_{TH} = V_{OD}$
- If #1: $W_{M0} \gg W_{M1}$
- If #2: M0 device is a min. device with 100nA current → Vgs=Vth
- Linear region current equals saturation current
- Then: $V_{DS,M1} = V_{OD} \rightarrow K = \mu C_{ox} = \frac{2I_D}{W_{M1}/L_{M1} * V_{DS,M1}^2}$





Threshold measurement of NMOS and PMOS



Threshold measurement and mobility of NMOS and PMOS