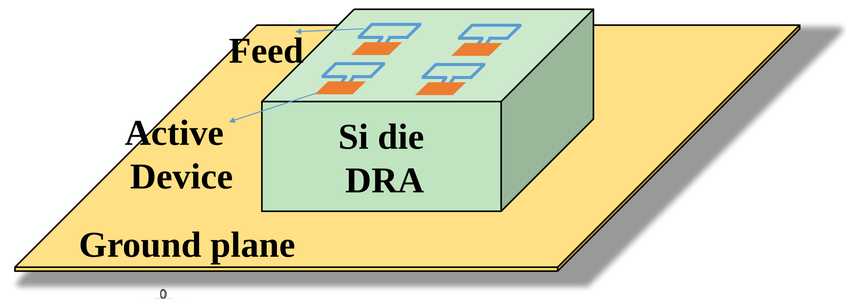
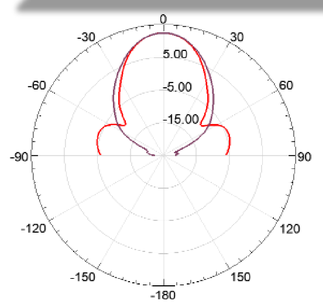
2020 Research Day

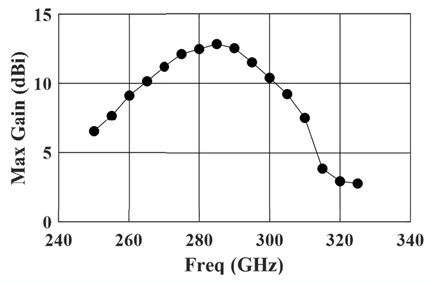
A 280GHz Chip Scale Dielectric Resonator Antenna with True Time Delay Beam Steering

Nadav Buadana, Samuel Jameson and Eran Socher

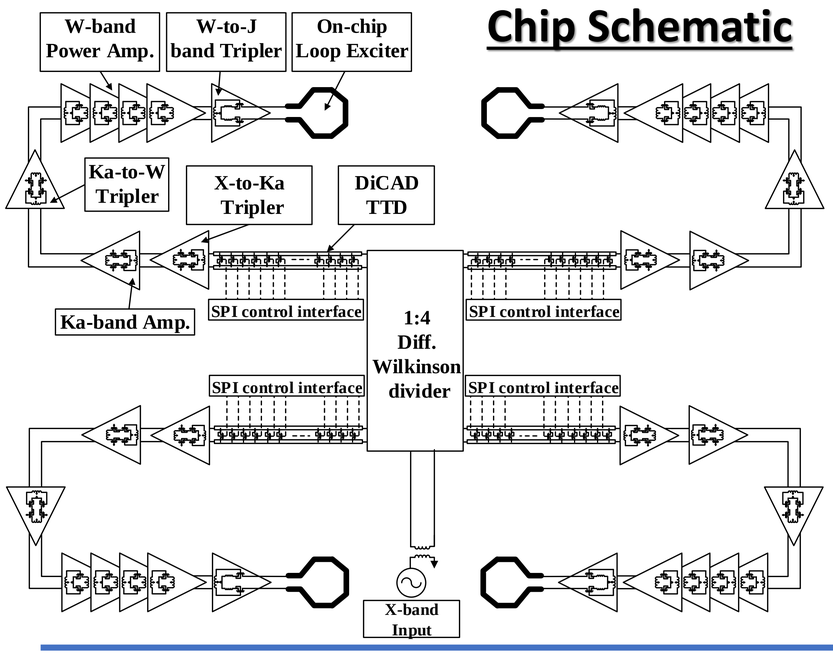
- CSDRA - A novel use of the silicon die as a rectangular Dielectric Resonator Antenna
- Power generation and excitation elements are integrated in standard 65nm CMOS process dies
- 4 channels with x27 Active Multiplying Chains (AMC)
- Individual DiCAD based True Time Delay to calibrate phase variations between channels and perform beam steering
- Top side radiation without any post-processing, external lens or superstrate



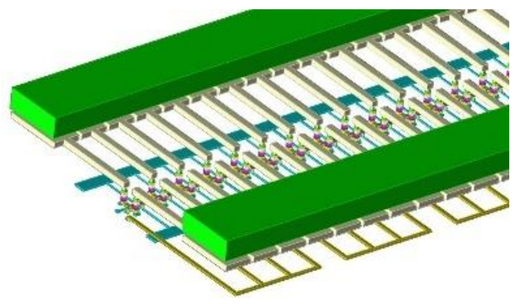


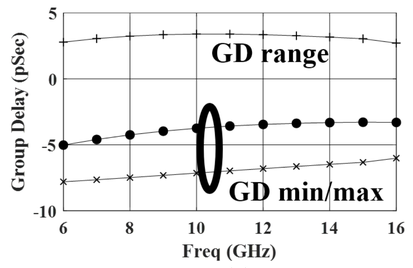


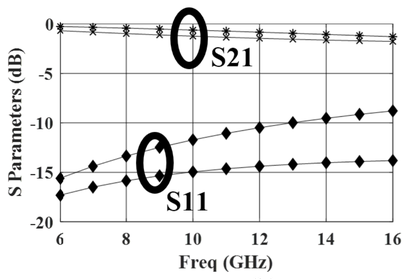
Chip Schematic



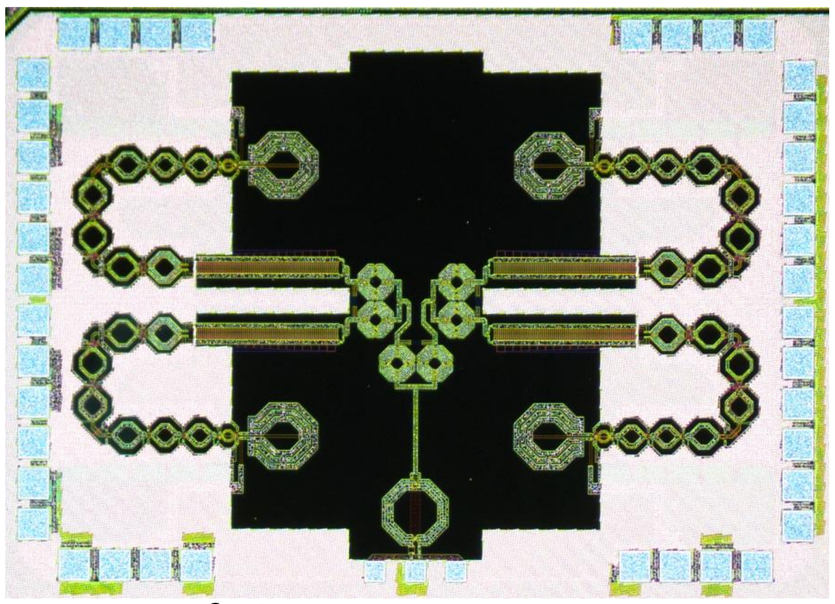
DiCAD TTD





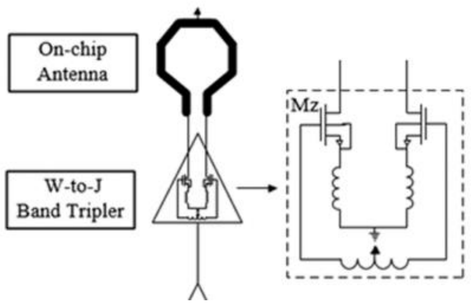


- DiCAD - Digitally Controlled Artificial Dielectric
- Short, switched metal strips increase only the odd mode capacitance
- Efficient way to modify the Effective Dielectric Constant (εr~Codd)
- High resolution, digitally controlled and low loss True Time Delay

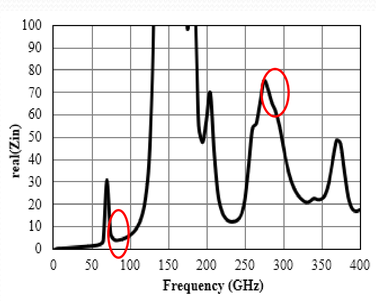


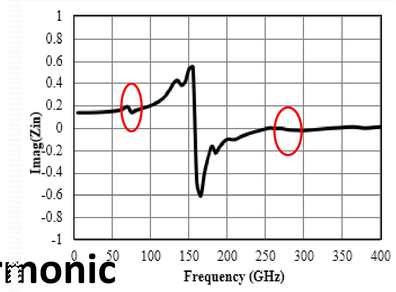
1.4x2 mm² die

Tri Function Loop



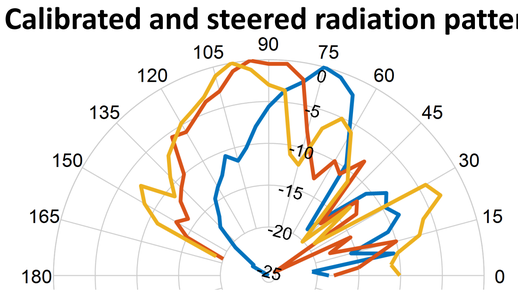
1. DC feed at virtual ground
2. Inductor at 1st harmonic
3. Exciting element at 3rd harmonic



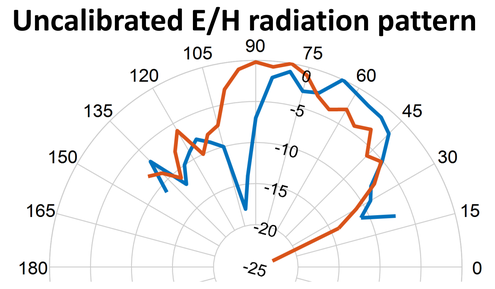


Experimental Results

Calibrated and steered radiation pattern

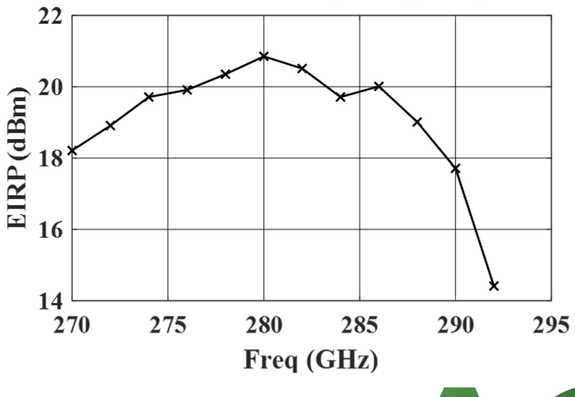


Uncalibrated E/H radiation pattern



Ref	Technology	Frequency	Architecture	Antenna	TRP	EIRP	P_{DC}	Eff.	Size	Power Density
Units		GHz			dBm	dBm	mW	%	mm²	mW/ mm²
TTST[8]	130nm SiGe	210-270	x16+Amp	Slot (DP)*	5	--	1600	0.19	3.2	1
JSSCC[7]	130nm SiGe	320	PLL Osc	Slot x 16*	3	21.5	600	0.33	2.1	0.95
TMTT[6]	45nm CMOS	370-410	x4	Patch x 8*	-7	8.5	1500	0.013	10.5	0.02
TMTT[5]	45nm CMOS	395-435	x4	Slot x 8*	-10	4	700	0.014	10.28	0.97
TTST[4]	65nm CMOS	280-296	x27	Loop	0	10.2	284	0.34	0.49	2
ISSCC[9]	130nm SiGe	317	PLL Osc	Slot	0.9	13.9	610	0.2	2.1	0.58
This work	65nm CMOS	272-288	x27	CSDRA	8.5	21	980	0.72	2.8	2.253

Maximum EIRP vs, Freqyency



Measured vs. Simulated Gain