2020 Research Day

An 88fJ / 40 MHz [0.4V] – 0.61pJ / 1GHz [0.9V] Dual Mode Logic 8x8 bit Multiplier Accumulator with a Self-Adjustment Mechanism in 28nm FD-SOI

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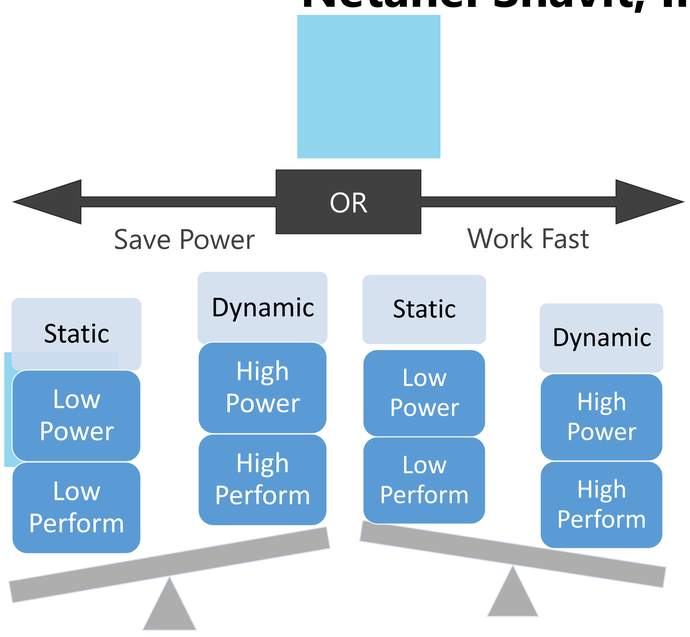
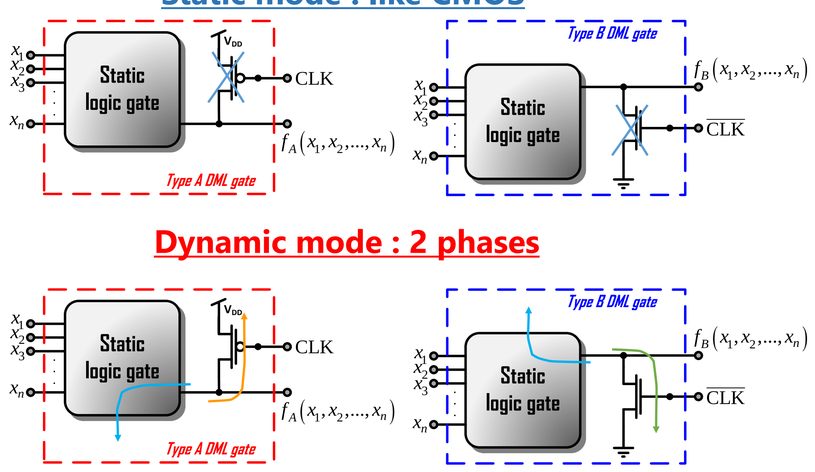
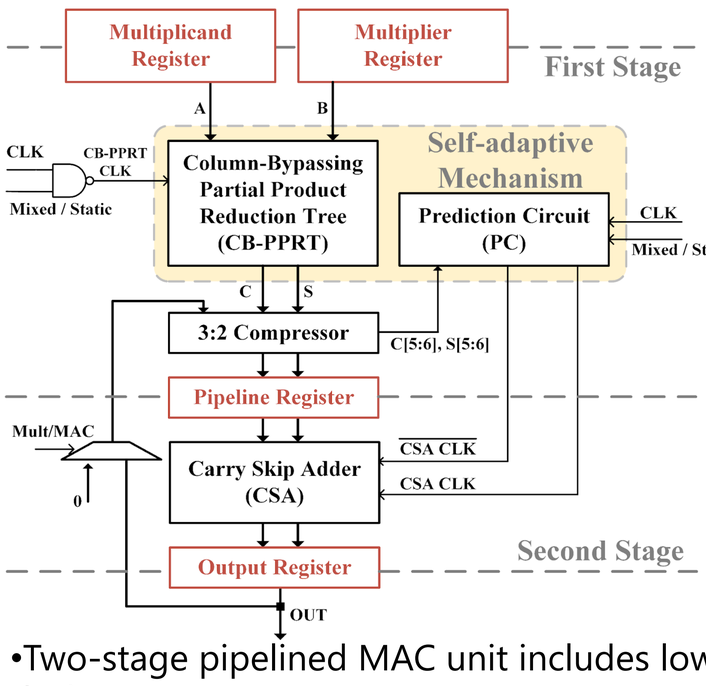


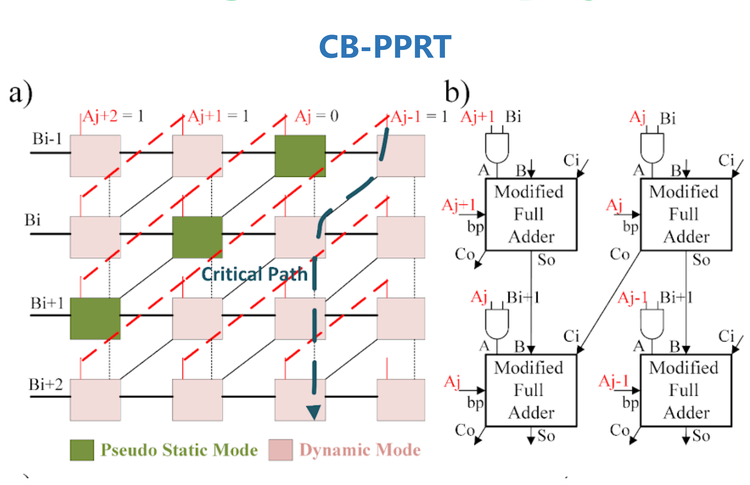
Dual Mode Logic



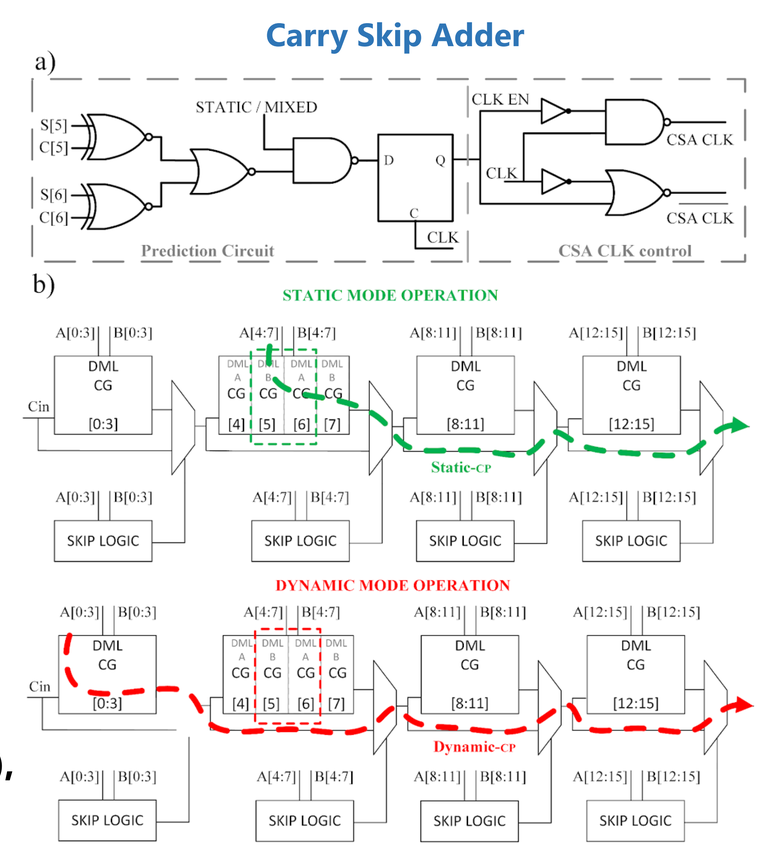
- Dual Mode Logic offers two different operation modes.
- **Static mode**: DML gates exhibit very low energy consumption with reduced performance.
- **Dynamic mode:** achieves high speed and high energy consumption.
- Operation modes (static and dynamic) can be combined (mixed mode) within the same design for an optimal energy-delay (E-D) tradeoff.
- DML can switch between operating modes on-the-fly according to the system requirements.

Dual Mode Logic Multiply Accumulate





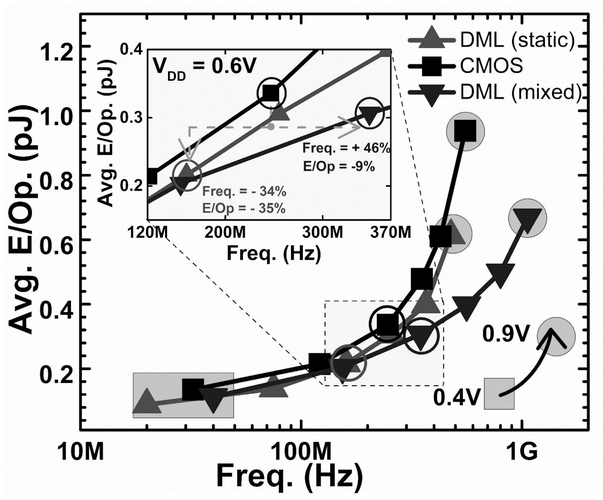
(a) Combined static and dynamic operations of the DML CB-PPRT in the mixed-mode operation. (b) Sketch of a group of FA cells.



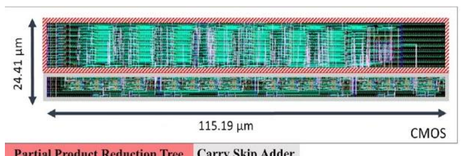
(a) Schematics of the Predictor and the critical path of the DML CSA operating in the (b) static mode and (c) dynamic mode.

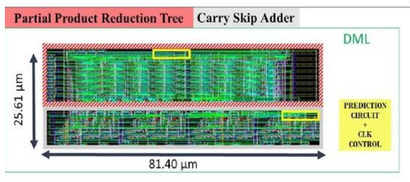
- Two-stage pipelined MAC unit includes low-complexity extra clock control, required for the DML design.
- The first stage originates from the **column bypassing partial product reduction tree (CB-PPRT),** re-designed for the proposed DML-based architecture.
- Second stage, the **DML carry-skip adder (CSA)** produces the final output.

Measurement Results

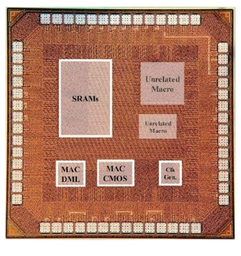


Average E/Op versus frequency for *V*DD ranging from 0.4 to 0.9 V (α = 0.3).





Layouts of the compared designs



Micrograph of the testchip with DML and CMOS MACs

Conclusions

8 X 8 bit DML MAC

-35%	+46%	-25%
Energy	Frequency	Area

- DML gates to operate either in the static or dynamic mode to provide E-D optimization at run time.
- The mixed mode leads to improvements in both speed and energy for a wide range of supply voltages.
- Comparative measurement results show that the DML MAC outperforms its CMOS counterpart.

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