2020 Research Day

Replica Bit-Line Technique for Internal Refresh in Logic-Compatible Gain-Cell Embedded DRAM

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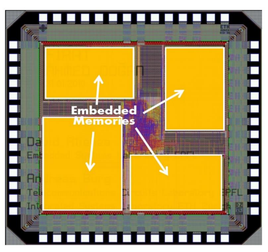
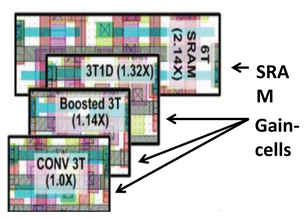
Motivation

- Increasing need for embedded memories in SoCs & ASICs
- Memories often consume > 50% of area & power
- 1st point of failure under voltage scaling



Advantages of GC-eDRAM Technology

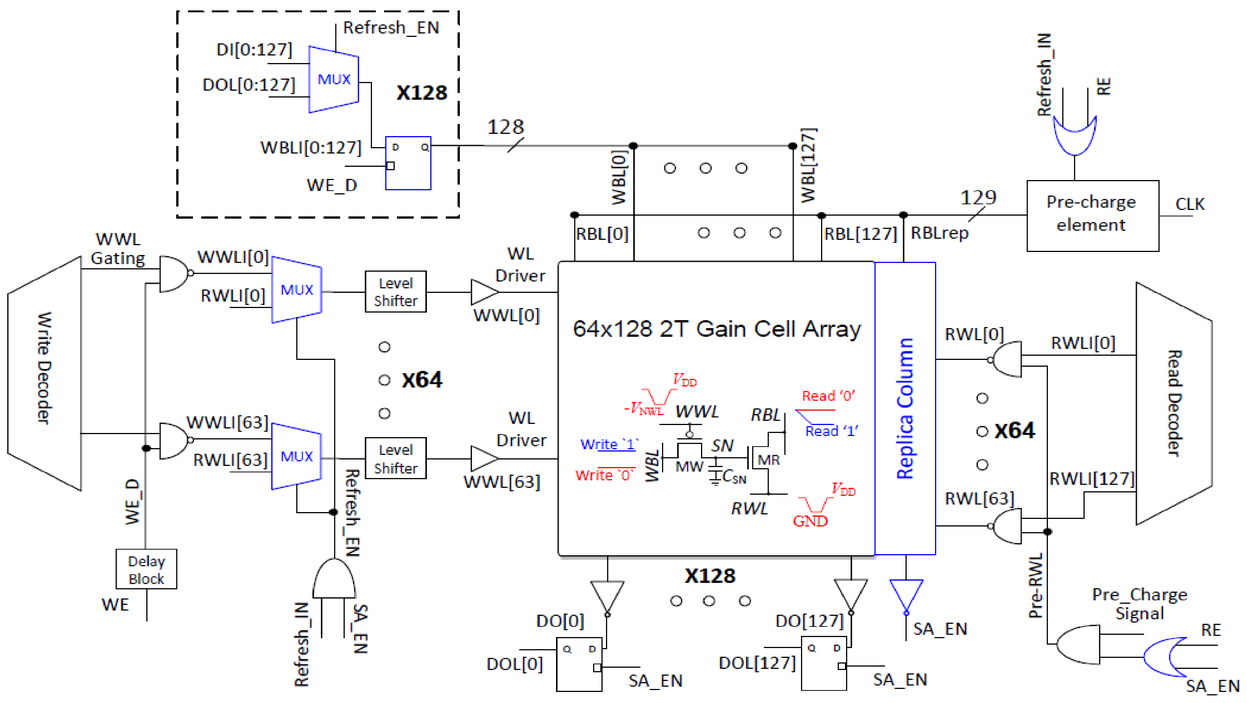
- Smaller cell size than SRAM, less bitcell leakage
- Logic-compatible (no special process steps).
- Naturally two-ported: Optimize for read & write.
- Can have lower retention power than SRAM.

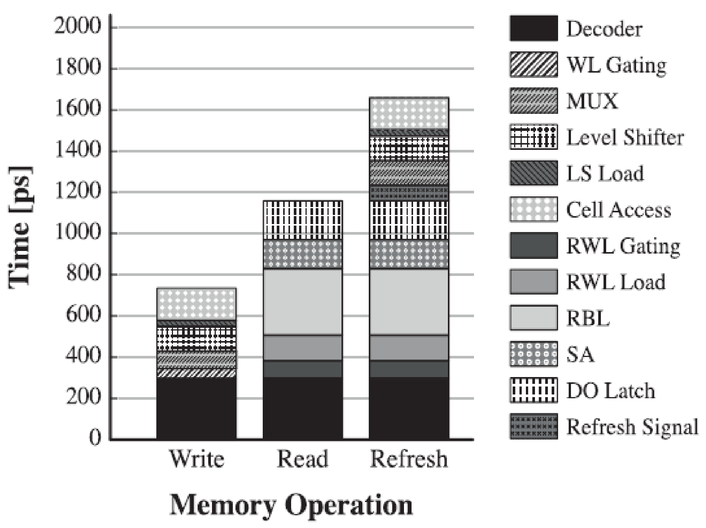


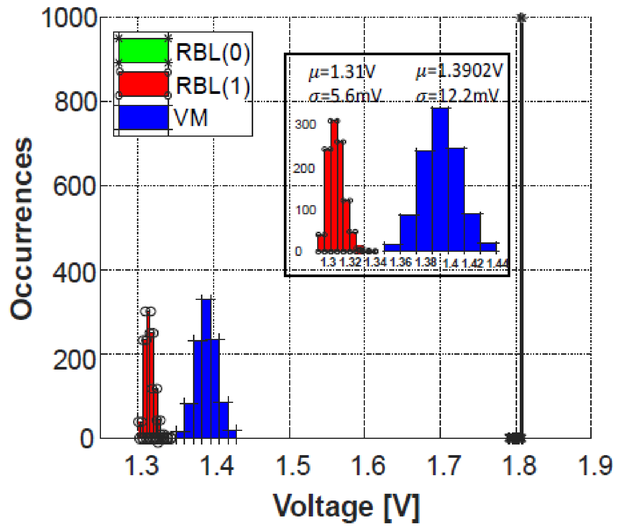
Gain-Cell Drawbacks

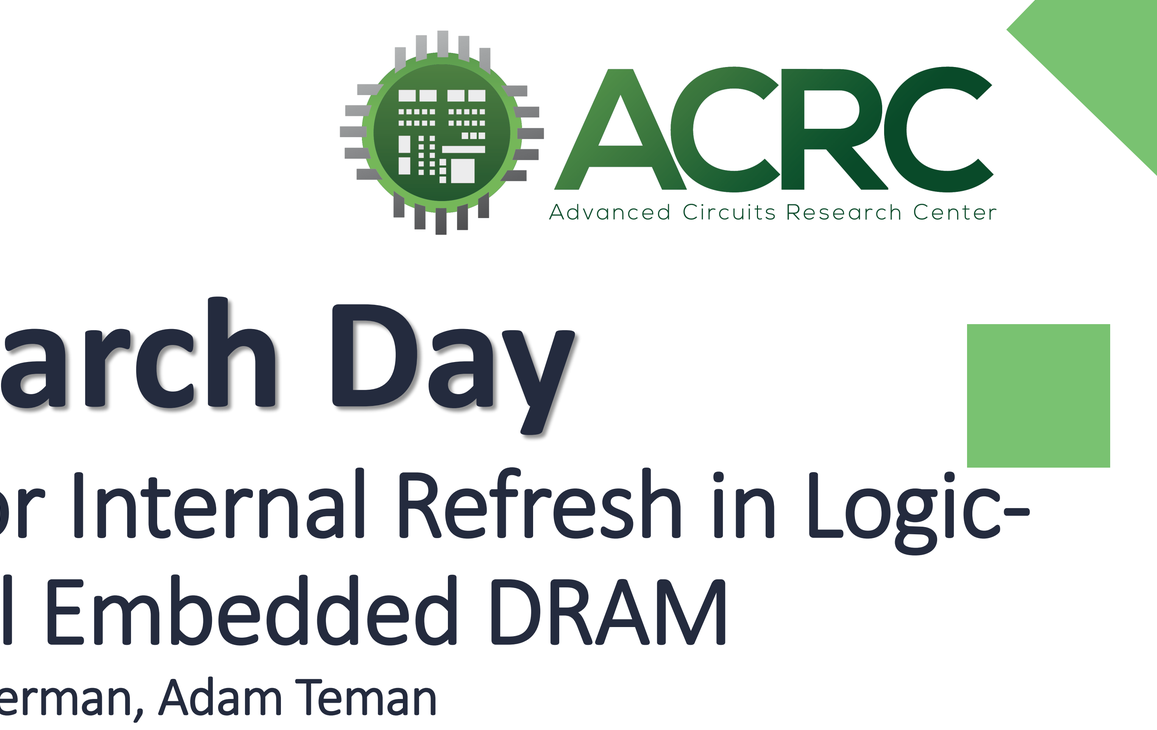
- Requirement of periodic refresh cycles.
- Large variability of retention time - global refresh rate is determined by the worst cell.
- During the refresh cycles we can not necessarily access the cell to read and write.

Memory Macro Architecture









Refresh Unit

- GC-eDRAM requires periodic refresh cycles to maintain its data.
- The refresh operation is usually handled at an architecture level by reading out and writing back the entire memory array every refresh cycle.
- An external refresh unit results in a high power overhead and limited memory availability.
- We propose a new approach for the realization of the refresh operation, using and internal refresh mechanism and implemented in a circuit-level custom design.
- We use a dedicated replica column for tracking the RBL delay by using similar 2T cells which track the PVT variations.
- The SNs of the replica column are connected to a predefined reference voltage so that the RBL drives the dynamic sense amplifier for a correct read.

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