2020 Research Day

Disruptive Register Files for a Translation Lookaside Buffer (TLB)

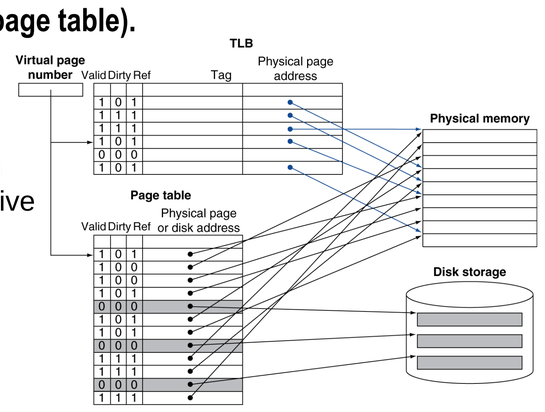
Introduction And Motivation

Collaboration between Dr. Teman's group and Dolphin Integration

Project Goal:

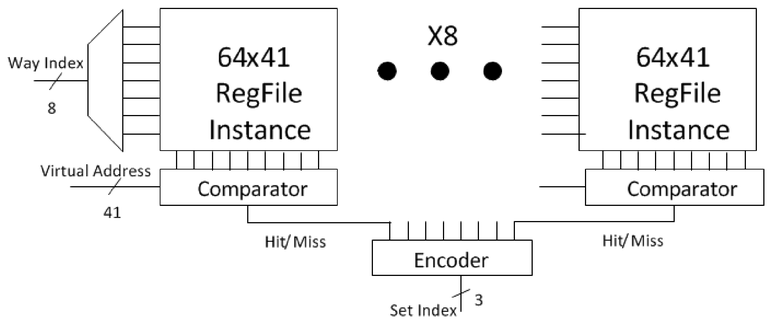
Development of a high-speed register file that will be used as a part of a Translation Lookaside Buffer (TLB)

- **A Translation Lookaside Buffer (TLB) is basically a cache of virtual to physical address translations (page table).**
  - A TLB is a subset of the page table that is stored on chip.
  - If a virtual address translation is in the TLB, it saves expensive DRAM accesses.
- **TLBs require high associativity to increase hit rate.**
  - Reduce conflict misses



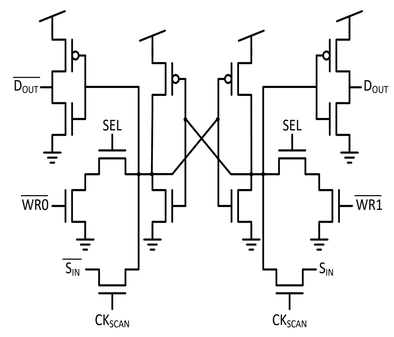
TLB Register File Spec

- **TLB Size: 512 Entry, 8-way Set Associative (64 sets) TLB**
- **Critical Path: Mux ctrl signals which propagate the entire width of the array**
- **Timing Target: 400ps for Read operation + Comparison + 1 MUX stage (PA array)**

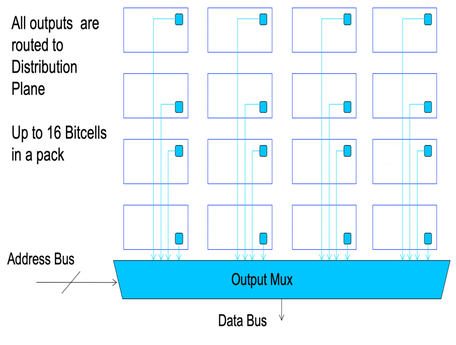


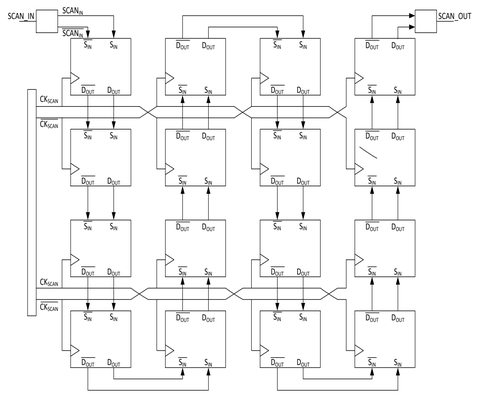
The basic Cell – "CARME"

- **Why CARME?**
  - Support for multiple high-speed read ports (static)
  - High - speed write
  - Resetable (global reset)
  - Scannable (chip testing - ATPG)



Array Architecture





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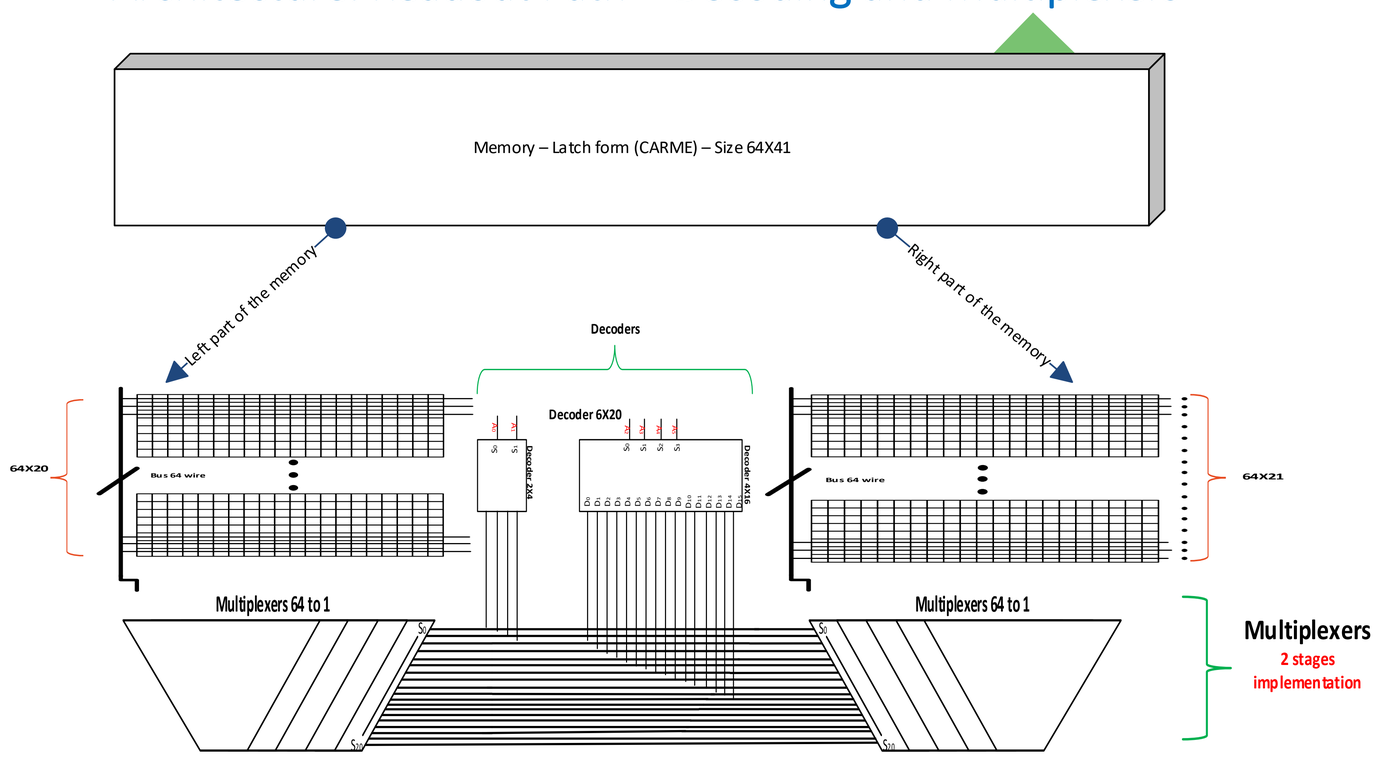
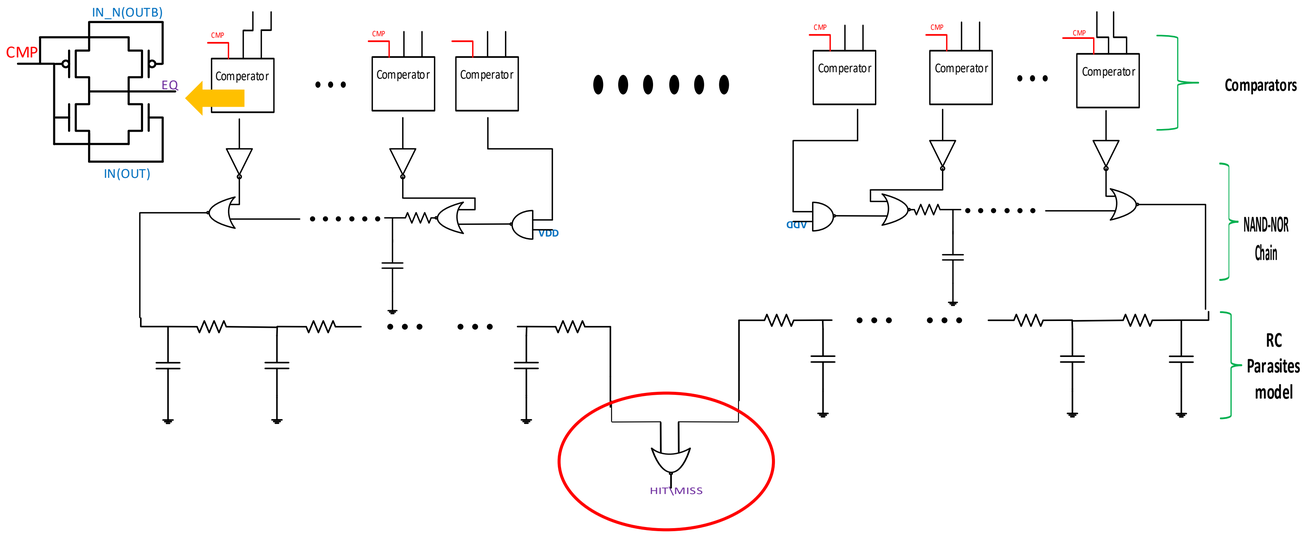
Architecture: Readout Path – Decoding and Multiplexers



Comparison + Chain to Hit/Miss



Performance at 16FFC Technology

Property/Challenge	Synthesizable FF-Based	Synthesizable Latch-Based	SRAM-Based	CARME Register
Area	1X	0.5X	0.35X	0.7X
Speed (access time, typical)	1X	1.5-2X	~2.5X	**~0.65X**
Power @1GHz	1X	0.4X	0.7X	0.45X
Reset	Yes	Yes	No	Yes
Write access	Synchronous	Synchronous	Synchronous	Synchronous
Read access	Asynch.	Synchronous	Synchronous	Asynch.
Multi Port	Yes	Yes	No	Yes

Comparison with Synthesized Register File

Property/Challenge	READ_ADDR1 -> HIT Worst Timing path: [ns]
Synthesizable FF-Based 1) No ratio	0.441 ns
Synthesizable FF-Based 2) Ratio 1.5	0.449 ns
Synthesizable FF-Based 3)Ratio 5	0.481 ns
Synthesizable FF-Based 4)Ratio 8	0.502 ns
Synthesizable FF-Based 4)Ratio 10	0.546 ns
CARME	0.340 ns

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